

Edgecore AS5915-18X
CPLD/FPGA Specification
Version: V0.3

Revision History

[illegible]

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1. LEDs

1.1.1. Network / Timing LEDs

The status of port LED will not be affected when the switch is in configuration mode. Each port has its dedicated LED with SFP+, SFP cage/connectors and RJ45 jack. The management port has dedicated LED to indicate Link and Activity. The ToD and BITS ports have dedicated LED to indicate Link status.

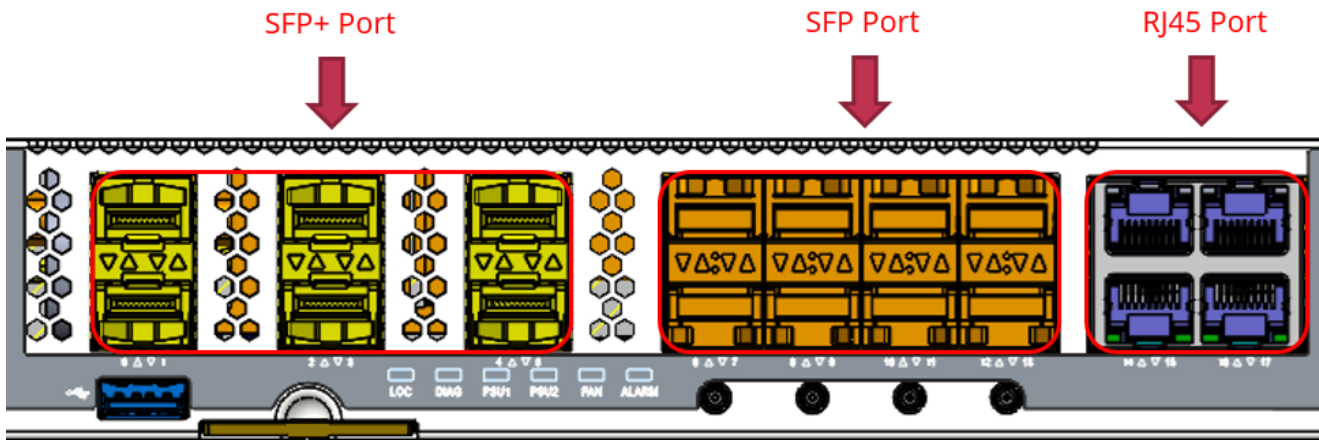


Figure 1 Network and Timing Port LEDs

LED	CONDITION	STATUS
SFP+ Port LED (Port0 to Port5) (Link)	On/Green	SFP+ port has a valid link and the solid green to indicate link.
	Off	There is no link on the port.
SFP+ Port LED (Port0 to Port5) (Activity)	Flashing/Green	SFP+ port has a valid activity at 10G mode and the flashing green to indicate 10G activity.
	Flashing/Amber	SFP+ port has a valid activity at 1G mode and the flashing blue to indicate 1G activity.
	Off	There is no activity on the port.
SFP Port LED (Port0 to Port 7) (Link)	On/Green	SFP port has a valid link and the solid green to indicate link.
	Off	There is no link on the port.
SFP Port LED (Port0 to Port7) (Activity)	Flashing/Green	SFP port has a valid activity at 1G mode and the flashing green to indicate 1G activity.
	Flashing/Amber	SFP port has a valid activity at 2.5G mode and flashing green to indicate 2.5G activity.

	Off	There is no activity on the port.
RJ45 Port LED (Port0 to Port3) (Link)	On/Green	Port has a valid link
	Off	There is no link on the port.
RJ45 Port LED (Port0 to Port3) (Activity)	Flashing/Green	Flashing indicates activity.
	Off	There is no activity on the port.
MGMT Port LED (Link)	On/Green	Port has a valid link
	Off	There is no link on the port
MGMT Port LED (Activity)	Flashing/Green	Flashing indicates activity
	Off	There is no activity on the port
ToD Status LED	On/Flashing Green	ToD port has an activity and the flashing to indicate activity.
	Off	There is no link on the port
BITS Status LED	On/Flashing Green	Bits port has an activity and the flashing to indicate activity.
	Off	There is no link on the port

Table 1 Port LED Definition

1.1.2.System LEDs

The system LEDs are used to indicate the status of power and system.

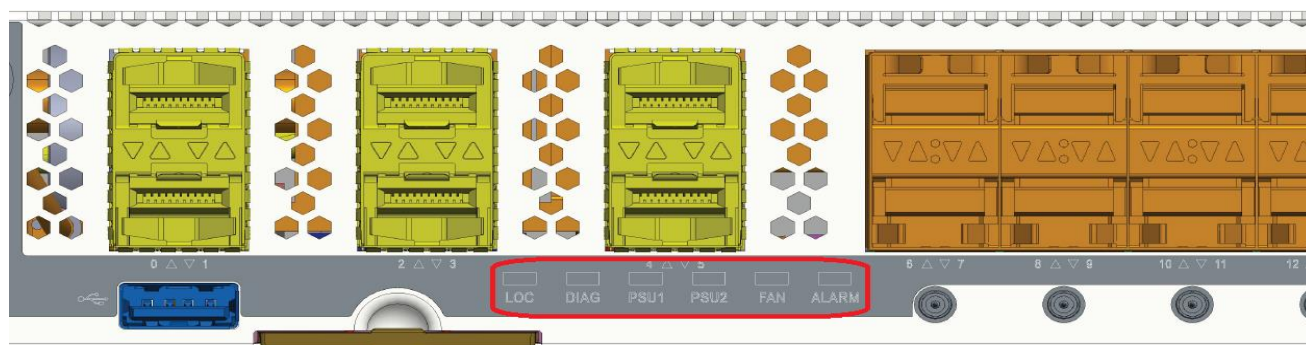


Figure 2 System LEDs

LABEL	COLOR	DESCRIPTION
PSU1 (PSU outputs 12V from 1 st DC input connector)	Green	This 12V is operating normally.
	Amber	PWR present but not power on or this power is fault.
	Off	Power supply not present.
PSU2 (PSU outputs 12V from	Green	This 12V is operating normally.
	Amber	PWR present but not power on or this power is fault.

2 nd DC input connector)	Off	Power supply not present.
DIAG (Diagnostic)	Green	System self-diagnostic test successfully completed.
	Green Blink	System self-diagnostic test is in progress
	Amber	System self-diagnostic test has detected a fault.
FAN	Green	System fans operating normally.
	Green Blink	System fans are power off when ambient temperature is less than 10 degree C.
	Amber	System FAN tray present but is fault.
ALRM	Green	System Alarm port operating normally.
	Red	System Alarm port is fault.
LOC	Blue Flashing	Flashing by remote management command. Assists the technician in finding the right device for service in the rack.
	OFF	Not a particular switch that technician need to find

Table 2 System LED Definition

1.2. Optical Modules Supported

The AS5915 system supports 6x 10G SFP+ ports, 8x 1G SFP ports on the front panel. The SFP+ ports can support speeds of 10Gbps full duplex. The SFP ports can pass traffic up to 1Gbps or 2.5Gbps speed.

The table below lists the optical types that will be qualified by the AS5915 customer. The AS5915 can support additional type of optics; however, the optical module type for each specific vendor will have to be qualified to operate well with the AS5915 system. These optical modules must have their optical and electrical performance analyzed in a DVT and system test environment to ensure high reliability.

Speed	Standard
1G Port	1000Base-SX (SFP)
	1000Base-LX (SFP)
	1G BX

	1000Base-T
10G Port	10GBASE-SR (SFP+)
	10GBASE-CR (SFP+)
	10GBASE-LR (SFP+)
	10G BX
	10GBASE-T
	SFP+ Tibit micro OLT

Table 3 Types of Transceiver Supported

2. Motherboard CPLD and FPGA and Fan Control

This system totally has 1x CPLD and 1x FPGA.

1. The CPLD shows network port LEDs and detects transceiver status.
2. The CPLD handles fan speed adjustment and detects fan status.
3. The FPGA handles initialization of various devices such as Zarlink PLL and BITS FRAMER.

It can also pull reset lines on I2C busses. The FPGA has PCIe access to the CPU for configuration options. The FPGA is also responsible for controlling the timing system and various clocks go into and out of the FPGA.

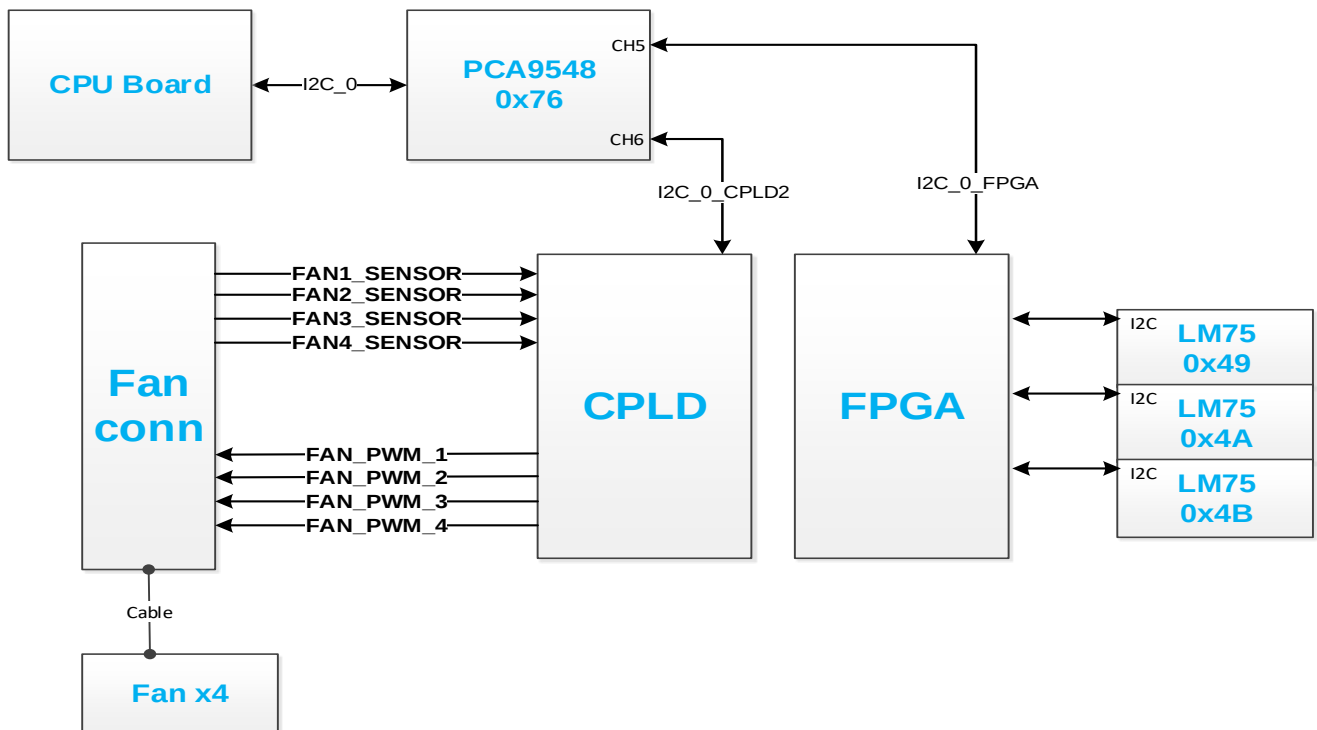


Figure 3 CPLD and FPGA

2.1.1.FPGA/CPLD Field upgrade information

The system supports SW field upgraded function for FPGA and CPLD on the motherboard. The FPGA and CPLD can be upgraded from the CPU using the USB to JTAG interface (this upgrade sequence goes over the FTDI component). There is only one image for the FPGA and CPLD. Once the images are upgraded, the entire AS5915 must be restarted for the new CPLD and FPGA images to be used. The 12V power rail can be hard reset using a

command from the CPU to the FPGA, and this can trigger a system restart after the operating system has verified that all upgrade is done.

2.1.2.FPGA

FPGA is on the motherboard with connections to CPU via I2C interface and I2C access address is 0x64. The following features are available with the FPGA:

- ~~D2D Margin High/Low control (only for test)~~
- Thermal sensor read/write
- PSU Power On/Off control
- Reset and Interrupt
- Interface translation (I2C to SPI)
- UART selection
- 1588 (currently supports TC without Boardsync interface.)

FPGA upgrade by JTAG that can through external connector or CPU, please see for detail block diagram.

2.1.3.FPGA PCIe Interface (Need to modify)

FPGA PCI BAR1 requests 512KB of memory. PCIe configuration register BAR0 determines the base address of these registers. Following table defines the base address of each major function in the FPGA.

Offset	Bit	Type	Default	Definition
0x0	[31:16]	RO	0x0000e001	Device ID.
	[15:0]	RO	0x00001172	Vendor ID.
0x04	[31:16]	RW		Status Register
	[15:0]	RW		Command register
0x08	[31:4]	RO	0x00200000	Class Code – simple communication controllers, others.
	[3:0]	RO	0x00000009	Revision ID.

0x0C	[31:24]	RO	0	BIST
	[23:16]	RO	0	Header Type
	[15:8]	RO	0	Latency Timer
	[7:0]	RO	0	Cache Line Status
0x10	[31:0]	RW	0xFFFF8,0000	BAR0, 512KB memory allocation.
0x14	[31:0]	RW	0	BAR1
0x18	[31:0]	RW	0	BAR2
0x1C	[31:0]	RW	0	BAR3
0x20	[31:0]	RW	0	BAR4
0x24	[31:0]	RW	0	
0x28			0	
0x2C	[31:16]	RO	0x00001144	Subsystem ID.
	[15:0]	RO	0x00001172	Subsystem Vendor ID.
0x30	[31:0]	RW	0	Expansion ROM Base Address
0x34	[31:4]	RO		Reserved
	[3:0]	RW		Capability Pointer.
0x38		RO		Reserved
0x3C	[31:24]	RO	0	Max Latency
	[23:16]	RO	0	Min Gnt.
	[15:8]	RO	0x01	Interrupt Pin.
	[7:0]	RO	0x00	Interrupt Line.

2.1.3.1. FPGA register

PCIe can use 0xdfxxxx00(Bar0)

Address(I2C)	Address(PCIe)	Register	R/W	Default value
0x00	0xdfxxxx00	PCB Version	Read Only	
0x01		FPGA version	Read Only	
0x02		Power module status	Read Only	
0x03		Power Enable	Read & Write	0x01
0x16	0xdfxxxx14	UART Select	Read & Write	0x00
0x20	0xdfxxxx20	Interrupt-1	Read Only	
0x21		Interrupt-1 Mask	Read & Write	0x00
0x22		Interrupt-2	Read Only	
0x23		Interrupt-2 Mask	Read & Write	0x00
0x24	0xdfxxxx24	Interrupt-3	Read Only	

Address(I2C)	Address(PCIe)	Register	R/W	Default value
0x25		Interrupt-3 Mask	Read & Write	0x00
0x26		Interrupt-4	Read Only	
0x27		Interrupt-4 Mask	Read & Write	0x00
0x30	0xdfxxxx30	Reset-1	Read & Write	0xFF
0x31		Reset-2	Read & Write	0xFF
0x32		Reset-3	Read Only	
0x33		Reset-4	Read & Write	0xFF
0x40	0xdfxxxx40	System LED-1	Read & Write	0xFF
0x41		System LED-2	Read & Write	0xFF
0x42		BITS LLP	Read Only	
0x50	0xdfxxxx50	Heater state	Read & Write	0x0F
0x60	0xdfxxxx60	Misc. control and state signals	Read & Write	0x25
0x70	0xdfxxxx70	I2C WDPLL Mux Control	Read & Write	0x00
0x71		10M Hz Mux Control	Read & Write	0x00
0x72		4K Hz Mux Control	Read & Write	0x00
0x73		1PPS Mux Control	Read & Write	0x00
0x80	0xdfxxxx80	I2C LM75 CPLD Mux Control	Read & Write	0x10
0x81		LM75_1 Temp Stored	Read & Write	0x00
0x82		LM75_2 Temp Stored	Read & Write	0x00
0x83		LM75_3 Temp Stored	Read & Write	0x00
0x86	0xdfxxxx84	FPGA I2C to UART & SPI Ctrl	Read & Write	0x03
0xA2	0xdfxxxxA0	TEST_LED_1	Read & Write	0xFE
0xA3		TEST_LED_2	Read & Write	0xFF
0xA4	0xdfxxxxA4	I2C Master Control	Read & Write	0x00
0xA5		Test ToD & UART	Read & Write	0x00
0xA8	0xdfxxxxA8	TEST_SMB_MODE	Read & Write	0x00
0xB0	0xdfxxxxB0	Scratch_Pad0	Read & Write	0xAA
0xB1		Scratch_Pad1	Read & Write	0xAA
0xB2		Scratch_Pad2	Read & Write	0x55
0xB3		Scratch_Pad3	Read & Write	0x55

Table 4 Register Address of PCIe Bar0

PCIe can use 0xdfxxxx00(Bar1)

Address(PCIe)	Register	R/W	Default value
0xdfxxxx00	PCB Version	Read Only	

Address(PCIe)	Register	R/W	Default value
...	FPGA version	Read Only	
0xdfxxxx3F	Power module status	Read Only	
	Power Enable	Read & Write	0x01
0xdfxxx1000	DC/DC Margin control-1	Read & Write	0x00
...	DC/DC Margin control-2	Read & Write	0x00
0xdfxxx1fff			

Table 5 Register Address of PCIe Bar1

PCIe can use 0xdfxxxx00(Bar2)

Address(PCIe)	Register	R/W	Default value
0xdfxxxx000	PCB Version	Read Only	
	FPGA version	Read Only	
...	Power module status	Read Only	
0xdfxxxx3FF	Power Enable	Read & Write	0x01

Table 6 Register Address of PCIe Bar2

PCIe can use 0xdfxxxx00(Bar3)

Address(PCIe)	Register	R/W	Default value
0xdfcxxxxx00	Read System ID	Read Only	0x000A7315

Table 7 Register Address of PCIe Bar3

The screenshot shows the 'System Contents' window with a list of components. The 'System ID Peripheral' component is selected, and its parameters are displayed on the right. The 'System ID' parameter is set to 0x000A7315. The 'Description' field contains the text: 'Please use hexadecimal numbers only in System ID.'

EX.

```
COM7 - Tera Term VT
File Edit Setup Control Window Help
root@(none):/# lspci -s 04:00.0 0x04.B=0x7
root@(none):/# lspci -vv -s 04:00.0
04:00.0 2000: 1172:e001 (rev 09)
Subsystem: 1172:1144
Control: I/O+ Mem+ BusMaster+ SpecCycle- MemWINV- VGASnoop- ParErr- Stepping- SERR+ FastB2B- DisINTx-
Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort- >SERR- <PERR- INTx-
Latency: 0, Cache Line Size: 64 bytes
Interrupt: pin A routed to IRQ 15
Region 0: Memory at dfc0b000 (32-bit, non-prefetchable) [size=1K] Bar0
Region 1: Memory at dfc08000 (32-bit, non-prefetchable) [size=8K] Bar1
Region 2: Memory at dfc0a000 (32-bit, non-prefetchable) [size=1K] Bar2
Region 3: Memory at dfc00000 (32-bit, non-prefetchable) [size=32K] Bar3
Capabilities: [50] MSI: Enable- Count=1/1 Maskable- 64bit+
Address: 0000000000000000 Data: 0000
Capabilities: [78] Power Management version 3
Flags: PMEClk- DSI- D1- D2- AuxCurrent=0mA PME(D0-,D1-,D2-,D3hot-,D3cold-)
Status: D0 NoSoftRst- PME-Enable- DSel=0 DScale=0 PME-
Capabilities: [80] Express (v1) Endpoint, MSI 00
DevCap: MaxPayload 128 bytes, PhantFunc 0, Latency L0s <64ns, L1 <1us
ExtTag- AttnBtn- AttnInd- PwrInd- RBE+ FLReset- SlotPowerLimit 10.000W
DevCtl: Report errors: Correctable+ Non-Fatal+ Fatal+ Unsupported-
RlxdOrd+ ExtTag- PhantFunc- AuxPwr- NoSnoop+
MaxPayload 128 bytes, MaxReadReq 512 bytes
DevSta: CorrErr- UncorrErr- FatalErr- UnsuppReq- AuxPwr- TransPend-
LnkCap: Port #1, Speed 2.5GT/s, Width x1, ASPM L0s, Exit Latency L0s unlimited
ClockPM- Surprise- LLActRep- BwNot- ASPMOptComp-
LnkCtl: ASPM Disabled; RCB 64 bytes Disabled- CommClk-
ExtSynch- ClockPM- AutWidDis- BWInt- AutBWInt-
LnkSta: Speed 2.5GT/s, Width x1, TrErr- Train- SlotClk+ DLActive- BWMgmt- ABWMgmt-
Capabilities: [100 v1] Virtual Channel
Caps: LPEVC=0 RefClk=100ns PATEntryBits=1
Arb: Fixed+ WRR32- WRR64- WRR128-
Ctrl: ArbSelect=Fixed
Status: InProgress-
VC0: Caps: PATOffset=00 MaxTimeSlots=1 RejSnoopTrans-
Arb: Fixed- WRR32- WRR64- WRR128- TWRR128- WRR256-
Ctrl: Enable+ ID=0 ArbSelect=Fixed TC/VC=01
Status: NegoPending- InProgress-
lspci: Unable to load libkmod resources: error -12
root@(none):/#
```

2.1.3.2. Offset 0x00 PCB Version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:2	(Reserved)			
1:0	PCB_version[2:0] [PCB_Ver_3, Ver_2, Ver_1]	R	000	001: R0A 010: R0B 011: R0C 100: R0D 101: R01 Others: Reserved

2.1.3.3. Offset 0x01 FPGA version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	CPLD_ver[7:0]	R	000	[7:2]: Reserved [1:0]: CPLD version

2.1.3.4. Offset 0x02 Power module status (Read&Write)

Bit	Name	R/W	Reset Value	Description
7	PS2_ON	R/W	0	0: PSU2 12V output 1: PSU2 12V no output
6	PS1_ON	R/W	0	0: PSU1 12V output 1: PSU1 12V no output
5	PS2_AC_ALERT	R	1	0: PSU2 POWER Fail 1: PSU2 POWER Good
4	PS1_AC_ALERT	R	1	0: PSU1 POWER Fail 1: PSU1 POWER Good
3	PS2_12V_PG	R	1	0: PSU2 12V Power Fail 1: PSU2 12V Power Good
2	PS1_12V_PG	R	1	0: PSU1 12V Power Fail 1: PSU1 12V Power Good
1	RESET_PSU_I2C_2	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
0	RESET_PSU_I2C_1	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state

2.1.3.5. Offset 0x03 Power Enable (Read&Write)

Bit	Name	R/W	Reset Value	Description
7:1	(Reserved)	R/W	0	
0	USB_PWRON_N	R/W	1	0: USB HUB power converter disable 1: USB HUB power converter enable

2.1.3.6. Offset 0x16 UART select (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	Reserved	N/A		
6	GPS_RX or CPU_TX(FPGA1588_TOD_OUT_R) to FPGA1588_UART1_TOD_OUT	R/W	0	0: Switch FPGA1588_TOD_OUT_R to output. 1: Switch GPS_UART_RX_R to output.
5	FPGA_SN65C_2DE	R/W	0	0: Switch TOD_RJ45 as input. 1: Switch TOD_RJ45 as output.
4	FPGA_SN65C_1DE	R/W	0	0: Switch 1pps to input. (not define) 1: Switch 1pps to output. (not define)
3:2	GPS_UART_RX_R (ToD_GPS) GPS_UART_RJ_RX (ToD_RJ45)	R/W	00	00: select GPS as UART input to the CPU. 01: select ToD_RJ45 as UART input to the CPU.
1:0	CPLD_RJ_UART_RX_R (RJ45) CPLD_USB_UART_RX_R (USB)	R/W	01	00: select RJ45 as UART input to the CPU. 01: select USB as UART input to the CPU.

2.1.3.7. Offset 0x20 Interrupt-1 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	CPLD2_INT	R	1	0: Interrupt assert 1: Interrupt deassert
6	CPU_THERMALTRIP	R	1	0: Interrupt assert 1: Interrupt deassert
5	CPU_PROCHOT	R	1	0: Interrupt assert 1: Interrupt deassert
4	LM75BD3_INT	R	1	0: Interrupt assert 1: Interrupt deassert
3	LM75BD2_INT	R	1	0: Interrupt assert 1: Interrupt deassert
2	LM75BD1_INT	R	1	0: Interrupt assert 1: Interrupt deassert
0:1	Reserved			

2.1.3.8. Offset 0x21 Interrupt-1 Mask (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	CPLD2_INT_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable
6	CPU_THERMALTRIP_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable
5	CPU_PROCHOT_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable
4	LM75BD3_INT_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable
3	LM75BD2_INT_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable
2	LM75BD1_INT_Mask	R/W	0	0: System Interrupt function enable

				1: System Interrupt function disable
0:1	Reserved			

2.1.3.9. Offset 0x22 Interrupt-2 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	UCD90160_INT	R	1	0: Interrupt assert 1: Interrupt deassert
6	INT_MGMT_PHY_N	R	1	0: Interrupt assert 1: Interrupt deassert
5	MAC_CPLD_INT_L	R	1	0: Interrupt assert 1: Interrupt deassert
4	THERMAL_INT_L	R	1	0: Interrupt assert 1: Interrupt deassert
3	USB_PWRFLT_N	R	1	0: Interrupt assert 1: Interrupt deassert
2	ZL30773_INT_REQ	R	1	0: Interrupt assert 1: Interrupt deassert
1:0	Reserved			

2.1.3.10. Offset 0x23 Interrupt-2 Mask(Read& Write)

Bit	Name	R/W	Reset Value	Description
7	UCD90160_INT_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable
6	INT_MGMT_PHY_N_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable
5	MAC_CPLD_INT_L_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable
4	THERMAL_INT_L_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable
3	USB_PWRFLT_N_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable
2	ZL30773_INT_REQ_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable
1:0	Reserved			

2.1.3.11. Offset 0x24 Interrupt-3 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5	FAN_INT_L	R	1	0: Interrupt assert 1: Interrupt deassert
4	INT_DS26503_L(BITS)	R	1	0: Interrupt assert 1: Interrupt deassert
3	CPLD23_INT_CPU	R	1	0: Interrupt assert 1: Interrupt deassert
2	Reserved	N/A		N/A

1	USB1_PWRFAULT	R	1	0: Interrupt assert 1: Interrupt deassert
0	SYS_CPLD_INT_CPU	R/W	1	0: Interrupt assert 1: Interrupt deassert

2.1.3.12. Offset 0x25 Interrupt-3 Mask (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5	FAN_INT_L_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable
4	INT_DS26503_L_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable
3	CPLD23_INT_CPU_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable
2	Reserved	N/A		N/A
1	USB1_PWRFAULT_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable
0	SYS_CPLD_INT_CPU_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable

2.1.3.13. Offset 0x26 Interrupt-4 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:2	Reserved			
1	MAC_THERM_DIODE_ALERT	R	1	0: Interrupt assert 1: Interrupt deassert
0	MAC_THERM_DIODE_THERM	R	1	0: Interrupt assert 1: Interrupt deassert

2.1.3.14. Offset 0x27 Interrupt-4 Mask (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
1	MAC_THERM_DIODE_ALERT_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable
0	MAC_THERM_DIODE_THERM_Mask	R/W	0	0: System Interrupt function enable 1: System Interrupt function disable

2.1.3.15. Offset 0x30 Reset-1 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	I2C_CPU1_RESET_N (I2C device address 0x72)	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
6	I2C_CPU0_RESET_N (I2C device address 0x76)	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
5	PSU_MONITOR_RESET_N	R/W	1	1: The Device is in normal operating state

	(I2C device address 0x74)			0: The Device is in reset state
4:2	Reserved	N/A		N/A
1	SP09_P16_RESET_N (I2C device address 0x71)	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
0	SP01_P08_RESET_N (I2C device address 0x70)	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state

2.1.3.16. Offset 0x31 Reset-2 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	RST_BITS_DS26503_R	R/W	0	1: The Device is in normal operating state 0: The Device is in reset state
6	CPLD_RST	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
5:4	Reserved			
3	MAC_RESET_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
2	54140_PHY_RST_L	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
1	ZL30773_RST	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
0	USB_RESET_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state

2.1.3.17. Offset 0x32 Reset-3 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:5	(Reserved)	R/W	0	
4	Reset_button_RST	R	1	0: Button reset to CPLD. Indicates Reset Button had pushed. 1: Normal
3	Reserved	N/A		
2	SYS_SW_RST_N	R	1	0:Indicate FPGA reset the system all of device ,system is in a reset state From CPU CB RESET.
1	Reserved	N/A		
0	POWER_RST	R	1	POWER_RST_S at FPGA IO D19. From UCD90160 GPIO11.

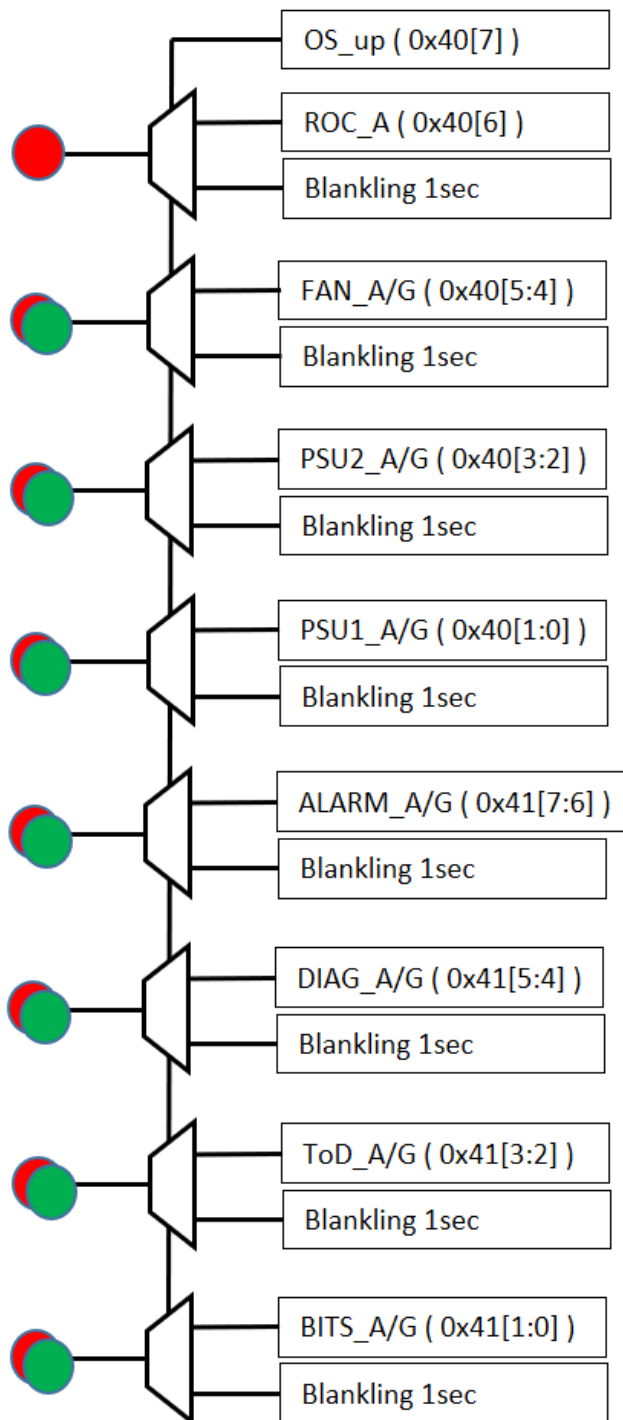
2.1.3.18. Offset 0x33 Reset-4 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved	N/A		N/A
4	GPS_RESET	R	1	1: The Device is in normal operating state 0: The Device is in reset state
3	UCD90610_RST	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
2	TPM_RESET_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
1	FT2232H_RESET_N(USB to	R/W	1	1: The Device is in normal operating state

	JTAG)			0: The Device is in reset state
0	8T49N240_OE	R/W	0	1: The Device is in normal operating state 0: The Device is in reset state

2.1.3.19. Offset 0x40 System LED-1 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	OS_up	R/W	1	0: All system LED will be blinking at 1Hz rate 1: All system LED can be controlled by register
6	LOC_A	R/W	1	0: Flashing by remote management command. Assists the technician in finding the right device for service in the rack. (show Amber blink) 1: Not a particular switch that technician need to find. (LED off)
5	FAN_G FAN_A	R/W	11	00: indicator light is off. 10: System FAN operating normally. 01: System FAN tray present but is fault. 11: Green blinking->System FAN tray is power on but not running due to low temperature (which means FAN is function OK) (Reserved)
4				
3	PSU2_G	R/W	0	0: indicator light is on when power good enable. 1: indicator light is off.
2	PSU2_A	R/W	1	0: indicator light is on when power good disable. 1: indicator light is off.
1	PSU1_G	R/W	0	0: indicator light is on when power good enable. 1: indicator light is off.
0	PSU1_A	R/W	1	0: indicator light is on when power good disable. 1: indicator light is off.



2.1.3.20. Offset 0x41 System LED-2 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	ALARM_G	R/W	0	0: LED blinking. 1: LED OFF
6	ALARM_A	R/W	1	0: LED ON. 1: LED OFF.
5:4	DIAG_G DIAG_A	R/W	11	00: System self-diagnostic test is in progress.(show Green Blink) 01: System self-diagnostic test successfully completed. (show Green) 10: System self-diagnostic test has detected a fault. (show Amber) 11: Diagnostic doesn't active.(LEDs are all off)
3	ToD_G	R/W	1	0: indicator light is on. (when ToD port enable) 1: indicator light is off.
2	ToD_A	R/W	1	0: LED ON. 1: LED OFF.
1	BITS_G	R/W	0	0: indicator light is on. (when LLP enable) 1: indicator light is off.
0	BITS_A	R/W	1	0: LED ON. 1: LED OFF.

2.1.3.21. Offset 0x42 BITS LLP (Read Only)

Bit	Name	R/W	Reset Value	Description
7:1	(Reserved)	R/W	0	
0	RLOS_FPGA	R	1	0: indicates that the LLP cable is inserted.

2.1.3.22. Offset 0x50 Heater state (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved	N/A		N/A
4	MB1_PWR_EN	R/W	1	1: Turn on DC12V switch 0: Turn off DC12V switch
3	Fan_idle	R	1	1: Fan normal operating 0: Fan stop operating
2:0	Reserved	N/A		N/A

2.1.3.23. Offset 0x60 Misc control and state signals (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	RESET_MAC88272	R	0	1: The Device is in normal operating state 0: The Device is in reset state
6	SW1_Select	R/W	0	0: CPU JTAG signals pass through to FPGA 1: CPU JTAG signals pass through to FAN CPLD
5	SYS_PWR_READY_R	R	1	1: Power sequence is ready. 0: Power sequence is not ready. From UCD90160 GPIO11
4:3	CPU_BIOS_DIS[1:0]	R/W	10	00 or 10: use dis0 flash to boot CPU 01 or 11: use dis1 flash to boot CPU
2	EE_WP	R/W	1	0:EEPROM write protect disable 1:EEPROM write protect enable
1	CPU_EEPROM_WP	R/W	1	0:EEPROM write protect disable 1:EEPROM write protect enable
0	UCD9090_ALERT_L	R/W	1	TBD To CPU GPI2.

2.1.3.24. Offset 0x70 I2C_WDPLL Mux Control

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2	I2C_MUX2_EN	R/W	0	0: internal cyclone4 i2c master to WAN_PLL_30773_SCL/SDA_FP 1: enable I2C1: WAN_PLL_82P30773_SCL/SDA to WAN_PLL that CPU can access WDPLL.
1:0	(Reserved)	R/W	0	

2.1.3.25. Offset 0x71 10MHz Mux Control (Reserved)

Bit	Name	R/W	Reset Value	Description
7:1	(Reserved)	R/W	0	
0	10M_SYNCE_FPGA_R (default) 10MHZ_WDPLL_1588_OUT_R_FPGA	R/W	1	0: Select sync-E as input to the SMB Conn out and MAC. 1: Select 1588 as input to the SMB Conn out and MAC.

2.1.3.26. Offset 0x72 4K Hz Mux Control (Reserved)

Bit	Name	R/W	Reset Value	Description
7:1	(Reserved)	R/W	0	
0	4K_SYNCE_FPGA_R(default) 4K_1588_FPGA_R	R/W	R/W	0: Select sync-E as input to MAC. 1: Select 1588 as input to MAC. Don't have input 4K clock to FPGA on schematic?

2.1.3.27. Offset 0x73 1pps Mux Control (Reserved)

Bit	Name	R/W	Reset Value	Description
7:4	(Reserved)	R/W	0	
3:2	FAP_NSE_SYNC_IN1(default) MAC_1PPS_IN_2 MAC_1PPS_IN_1	R/W	00	00: Select MAC_NSE_SYNC_IN1 as input to WDPLL and 1PPS_MAC_OUT_MUX 01: Select MAC_NSE_SYNC_OUT as input to WDPLL and 1PPS_MAC_OUT_MUX 10: Select MAC_GPIO1 as input to WDPLL and 1PPS_MAC_OUT_MUX
1:0	1PPS_SYNCE_1588_OUT_R_FPGA(default) 1PPS_WDPLL_1588_OUT_R_FPGA 1PPS_MAC_OUT_MUX	R/W	00	00: Select sync-E as input to SMB CONN and MAC 01: Select 1588 as input to SMB CONN and MAC 10: Select MAC as input to SMB CONN and MAC

2.1.3.28. Offset 0x80 I2C LM75 CPLD Mux Control (Reserved)

Bit	Name	R/W	Reset Value	Description
7:5	I2C_Channel_Sel	R/W	000	100: LM75BD3_SCLK U18 011: LM75BD2_SCLK U29 010: LM75BD1_SCLK U27 001: FAN_SCL_FPGA_R FAN_CPLD 0x66 000: I2C not selected Notice: When bit4 =1 recommend set bit7:5 to 3'b000
4	wI2cMasterEn	R/W	1	LM75B / FPGA to CPLD I2C Master / I2C_MUX2 Enable Control 1 : Enable FPGA to CPLD I2C Master & LM75B Temp IC I2C Master Disable I2C_MUX2

				(Automatic control) 0 : Disable FPGA to CPLD I2C Master & LM75B Temp IC I2C Master Enable I2C_MUX2 Notice: When bit4 =1 CPU can't access LM75B & FAN_CPLD (Manual control)
3:0	(Reserved)	R/W	0	

2.1.3.29. Offset 0x81 LM75_1 Temp Stored (Reserved)

Bit	Name	R/W	Reset Value	Description																																																
7:0	2's complement of Temp data	R	8'h00	7.4.3 Temperature register The Temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one Most Significant Byte (MSByte) and one Least Significant Byte (LSByte). However, only 11 bits of those two bytes are used to store the Temp data in 2's complement format with the resolution of 0.125 °C. Table 8 shows the bit arrangement of the Temp data in the data bytes. Table 8. Temp register <table><tr><th colspan="8">MSByte</th><th colspan="8">LSByte</th></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>D10</td><td>D9</td><td>D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr></table> Notice: Only store Temp Reg MSByte address:0x4C	MSByte								LSByte								7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X
MSByte								LSByte																																												
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0																																					
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X																																					

2.1.3.30. Offset 0x82 LM75_2 Temp Stored (Reserved)

Bit	Name	R/W	Reset Value	Description																																																
7:0	2's complement of Temp data	R	8'h00	7.4.3 Temperature register The Temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one Most Significant Byte (MSByte) and one Least Significant Byte (LSByte). However, only 11 bits of those two bytes are used to store the Temp data in 2's complement format with the resolution of 0.125 °C. Table 8 shows the bit arrangement of the Temp data in the data bytes. Table 8. Temp register <table><thead><tr><th colspan="8">MSByte</th><th colspan="8">LSByte</th></tr><tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr></thead><tbody><tr><td>D10</td><td>D9</td><td>D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr></tbody></table> Notice: Only store Temp Reg MSByte address:0x49	MSByte								LSByte								7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X
MSByte								LSByte																																												
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0																																					
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X																																					

2.1.3.31. Offset 0x83 LM75_3 Temp Stored (Reserved)

Bit	Name	R/W	Reset Value	Description																																																
7:0	2's complement of Temp data	R	8'h00	7.4.3 Temperature register The Temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one Most Significant Byte (MSByte) and one Least Significant Byte (LSByte). However, only 11 bits of those two bytes are used to store the Temp data in 2's complement format with the resolution of 0.125 °C. Table 8 shows the bit arrangement of the Temp data in the data bytes. Table 8. Temp register <table><tr><th colspan="8">MSByte</th><th colspan="8">LSByte</th></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>D10</td><td>D9</td><td>D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr></table> Notice: Only store Temp Reg MSByte address:0x4A	MSByte								LSByte								7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X
MSByte								LSByte																																												
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0																																					
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X																																					

2.1.3.32. Offset 0x86 FPGA I2C to UART & SPI Ctrl (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	GPS module select	R/W	1	1:UbloX module 0:Trimble module
6:4	Reserved	N/A	000	
3	ToD_RX (GPS_UART_RJ_RX) Control	R/W	0	0: FIFO not save ToD_RX in
2	GPS_RX (GPS_UART_RX_R) Control	R/W	0	0: FIFO not save GPS_RX in
1	I2C_to_UART Controller Module Reset control	R/W	1	0: Reset I2C_to_UART Controller module
0	I2C_to_SPI Module Reset control I2C_to_UART Module Reset control	R/W	1	0: Reset iic_to_spi & iic_to_uart module

2.1.3.33. Offset 0xA2 TEST_LED_1 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	PSU2_A	R/W	1	When 0xA2 [0] = 1 (Test LED mode) 1: LED OFF 0: LED ON
6	PSU2_G	R/W	1	When 0xA2 [0] = 1 (Test LED mode) 1: LED OFF 0: LED ON
5	PSU1_A	R/W	1	When 0xA2 [0] = 1 (Test LED mode) 1: LED OFF 0: LED ON
4	PSU1_G	R/W	1	When 0xA2 [0] = 1 (Test LED mode) 1: LED OFF 0: LED ON
3	DIAG_A	R/W	1	When 0xA2 [0] = 1 (Test LED mode) 1: LED OFF 0: LED ON
2	DIAG_G	R/W	1	When 0xA2 [0] = 1 (Test LED mode) 1: LED OFF 0: LED ON
1	LOC_B	R/W	1	When 0xA2 [0] = 1 (Test LED mode) 1: LED OFF 0: LED ON
0	TEST LED Switch	R/W	0	0 : Normal mode 1 : Test LED mode

2.1.3.34. Offset 0xA3 TEST_LED_2 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	BITS_A	R/W	1	When 0xA2 [0] = 1 (Test LED mode) 1: LED OFF 0: LED ON
6	BITS_G	R/W	1	When 0xA2 [0] = 1 (Test LED mode) 1: LED OFF 0: LED ON
5	TOD_A	R/W	1	When 0xA2 [0] = 1 (Test LED mode) 1: LED OFF 0: LED ON
4	TOD_G	R/W	1	When 0xA2 [0] = 1 (Test LED mode) 1: LED OFF 0: LED ON
3	ALARM_R	R/W	1	When 0xA2 [0] = 1 (Test LED mode) 1: LED OFF 0: LED ON
2	ALARM_G	R/W	1	When 0xA2 [0] = 1 (Test LED mode) 1: LED OFF 0: LED ON
1	FAN_A	R/W	1	When 0xA2 [0] = 1 (Test LED mode) 1: LED OFF 0: LED ON
0	FAN_G	R/W	1	When 0xA2 [0] = 1 (Test LED mode) 1: LED OFF 0: LED ON

2.1.3.35. Offset 0xA4 I2C Master Control (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5	Generate 9 clock_2	R/W	0	1: Enable auto detect and send 9 SCL + 1 STOP when I2C hang up more than 800us 0: Disable
4	Auto Mode_2	R/W	0	1: Enable auto detect and send 9 SCL + 1 STOP when I2C hang up 0: Disable
3:2	Reserved			
1	Generate 9 clock_1	R/W	0	1: Enable auto detect and send 9 SCL + 1 STOP when I2C hang up more than 800us 0: Disable
0	Auto Mode_1	R/W	0	1: Enable auto detect and send 9 SCL + 1 STOP when I2C hang up 0: Disable

2.1.3.36. Offset 0xA5 Test ToD & UART (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	Reserved			
6	TEST_FPGA_1PPS_IN_TO_MUX	R		
5	TEST_GPS_CONN_1PPS_OUT	R		
4	TEST_FPGA_SN65C_2DE	R/W	0	0: Disenable 1: Enable output mode.
3	TEST_FPGA_SN65C_1DE	R/W	0	0: Enable receive mode. 1: Disenable.

2	TEST_GPS_CONN_1PPS_OUT_to_RJ	R/W	0	When Test mode enable and FPGA_SN65C_2DE =1: 0 : GPS_CONN_1PPS_OUT_to_Rjoutput low 1 : GPS_CONN_1PPS_OUT_to_Rjoutput high
1	TEST_FPGA1588_UART1_TOD_OUT	R/W	0	When Test mode enable and FPGA_SN65C_2DE=1: 0 : FPGA1588_UART1_TOD_OUT output low 1 : FPGA1588_UART1_TOD_OUT output high
0	TEST mode	R/W	0	1: enable 0: Disenable

2.1.3.37. Offset 0xA6 Control I2C Channel (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:2	Reserved			
2	Control ZL30773 I2C Master By PCIe Interface	R/W	0	0: Disable 1: Enable
1	ZL30773_I2C_Channel	R/W	0	0: control by 9548. 1: control by FPGA.
0	FAN_I2C_Channel	R/W	0	0: control by 9548. 1: control by FPGA.

2.1.3.38. Offset 0xA8 Test SMB (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	Test SMB Mode	R/W	0	0: SMB normal mode 1: SMB enter test mode
6:4	Reserved			
3	SMB_10MHz_IN	R		This bit represent current SMB_10MHz_IN status
2	SMB_1PPS_IN	R		This bit represent current SMB_1PPS_IN status
1	SMB_10MHz_OUT	R/W	0	When Test_SMB_Mode = 1, SMB_10MHz_OUT function as GPO to drive When Test_SMB_Mode =0, SMB_10MHz_OUT output SMB_10MHz_IN signal
0	SMB_1PPS_OUT	R/W	0	When Test_SMB_Mode = 1, SMB_1PPS_OUT function as GPO to drive When Test_SMB_Mode =0,

				SMB_1PPS_OUT output SMB_1PPS_IN signal
--	--	--	--	--

2.1.3.39. Offset 0xB0 Scratch_Pad0 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Scratch_Pad0	R/W	0xAA	This for SW R/W test

2.1.3.40. Offset 0xB1 Scratch_Pad1 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Scratch_Pad1	R/W	0xAA	This for SW R/W test

2.1.3.41. Offset 0xB2 Scratch_Pad2 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Scratch_Pad2	R/W	0x55	This for SW R/W test

2.1.3.42. Offset 0xB3 Scratch_Pad3 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Scratch_Pad3	R/W	0x55	This for SW R/W test

2.1.3.43. Offset 0xC0 Time_Step_1_RD (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[7:0]	R		This is for CRC function.

2.1.3.44. Offset 0xC1 Time_Step_2_RD (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[15:8]	R		This is for CRC function.

2.1.3.45. Offset 0xC2 Time_Step_3_RD (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[23:16]	R		This is for CRC function.

2.1.3.46. Offset 0xC3 Time_Step_4_RD (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[31:24]	R		This is for CRC function.

2.1.3.47. Offset 0xC4 Time_Step_5_RD (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[39:32]	R		This is for CRC function.

2.1.3.48. Offset 0xC5 Time_Step_6_RD (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[47:40]	R		This is for CRC function.

2.1.3.49. Offset 0xC6 Time_Step_7_RD (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[55:48]	R		This is for CRC function.

2.1.3.50. Offset 0xC7 Time_Step_8_RD (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[63:56]	R		This is for CRC function.

2.1.3.51. Offset 0xC8 Time_Step_9_RD (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[71:64]	R		This is for CRC function.

2.1.3.52. Offset 0xC9 Time_Step_10_RD (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[79:72]	R		This is for CRC function.

2.1.3.53. Offset 0xCA Accuracy_RD (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	CRC_Accuracy [7:0]	R		This is for CRC function.

2.1.3.54. Offset 0xCB CRC_RD (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	CRC[7:0]	R		This is for CRC function.

2.1.3.55. Offset 0xD0 Time_Step_1 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[7:0]	R/W	0x00	This is for CRC function.

2.1.3.56. Offset 0xD1 Time_Step_2 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[15:8]	R/W	0x00	This is for CRC function.

2.1.3.57. Offset 0xD2 Time_Step_3 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[23:16]	R/W	0x00	This is for CRC function.

2.1.3.58. Offset 0xD3 Time_Step_4 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[31:24]	R/W	0x00	This is for CRC function.

2.1.3.59. Offset 0xD4 Time_Step_5 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[39:32]	R/W	0x00	This is for CRC function.

2.1.3.60. Offset 0xD5 Time_Step_6 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[47:40]	R/W	0x00	This is for CRC function.

2.1.3.61. Offset 0xD6 Time_Step_7 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[55:48]	R/W	0x00	This is for CRC function.

2.1.3.62. Offset 0xD7 Time_Step_8 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[63:56]	R/W	0x00	This is for CRC function.

2.1.3.63. Offset 0xD8 Time_Step_9 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[71:64]	R/W	0x00	This is for CRC function.

2.1.3.64. Offset 0xD9 Time_Step_10 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	Time_Step[79:72]	R/W	0x00	This is for CRC function.

2.1.3.65. Offset 0xDA Accuracy (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	CRC_Accuracy [7:0]	R/W	0x00	This is for CRC function.

2.1.3.66. Offset 0xDB CRC (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	CRC[7:0]	R/W	0x00	This is for CRC function.

2.1.3.67. Offset 0xDC Boardsync_MISC(Read& Write)

Bit	Name	R/W	Reset Value	Description
7:1	Reserved			
0	Time stamp update[0]	R/W	0x00	1: update 0xD0~D9 0: close update

Cyclone4 FPGA I2C to UART & SPI Address mapping

I2C Address: 0x62 (7 bit) Offset address mode: 1 byte

SPI_BITS: SCLK: 1250000, CPOL=1, CPHA=1

UART_GPS : Core Speed: 38400 hz / Data Bit: 8bit / Parity: None / Stop Bit: 1bit /Not include CTS/RTS

UART_ToD : Core Speed: 38400 hz / Data Bit: 8bit / Parity: None / Stop Bit: 1bit /Not include CTS/RTS

FIFO_GPS: Depth:256

FIFO_ToD: Depth:256

Table 1.1. System Address mapping control by I2C slave to Avalon Master

	i2cslave_to_avlmm_bridge_0_avalon_master
mm_bridge_0_s0	
spi_0_spi_control_port	0x0000_0000 - 0x0000_001f
uart_gps_slave	0x0000_0020 - 0x0000_003f
uart_gps_read_fifo.in	0x0000_00a0 - 0x0000_00a3
uart_gps_read_fifo.out	0x0000_00a4 - 0x0000_00a7
uart_gps_read_fifo.in_csr	0x0000_0060 - 0x0000_007f
uart_tod.sl	0x0000_0040 - 0x0000_005f
uart_tod_read_fifo.in	0x0000_00b0 - 0x0000_00b3
uart_tod_read_fifo.out	0x0000_00b4 - 0x0000_00b7
uart_tod_read_fifo.in_csr	0x0000_0080 - 0x0000_009f

Table 1.2. SPI Master Core Address mapping control by I2C slave to Avalon Master

Internal Address	Register Name	Type [R/W]	32-11	10	9	8	7	6	5	4	3	2-0
0	rxdata ⁽⁸⁾	R	RXDATA (n-1..0)									
1	txdata ⁽⁸⁾	W	TXDATA (n-1..0)									
2	status ⁽⁶⁾	R/W			EOP	E	RRDY	TRDY	TMT	TOE	ROE	
3	control	R/W		SSO ⁽⁷⁾	IEOP	IE	IRRDY	ITRDY		ITOE	IROE	
4	Reserved	—										
5	slaveselct ⁽⁷⁾	R/W	Slave Select Mask									
6	eop_value ⁽⁸⁾	R/W	End of Packet Value (n-1..0)									

Table 1.3 Uart Master Core Address mapping control by I2C slave to Avalon Master

Offset	Register Name	R/W	Description/Register Bits													
			15:13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	rxdata	RO	Reserved					(2)	(2)	Receive Data						
1	txdata	WO	Reserved					(2)	(2)	Transmit Data						
2	status ⁽¹⁾	RW	Reserved	eop	cts	dcts		e	rrdy	trdy	tmt	toe	roe	brk	fe	pe
3	control	RW	Reserved	ieop	rts	idct s	trbk	ie	irrd y	itrd y	itmt	itoe	iroe	ibrk	ife	ipe
4	divisor ⁽³⁾	RW	Baud Rate Divisor													
5	endof- packet ⁽³⁾	RW	Reserved					(2)	(2)	End-of-Packet Value						

Table 1.4 FIFO CSR register Address mapping control by I2C slave to Avalon Master

offset	31				24	23					16	15					8	7	6	5	4	3	2	1	0										
base	fill_level																																		
base + 1																					i_status														
base + 2																					event														
base + 3																					interrupt enable														
base + 4	almostfull																																		
base + 5	almostempty																																		

I2C to Uart Command Example

1. I2C write data to UART GPS TX flow

i2c read addr:0x62 offset :0x28(status) → Check offset 0x28 bit 5(TOE) , 6(ROE) is equal to 1 or not

i2c write addr:0x62 offset :0x24(txdata) Data:0xFF → UART TX Send 0xFF to GPS RX

2. i2c read data from UART GPS RX flow

i2c read addr:0x62 offset :0x64(status) bit 1 → Check offset 0x64 bit0 is equal to 1 or not

i2c read addr:0x62 offset :0xA4(fifo.out) → Read data from fifo output data is gps tx data\

3. i2c read data from UART ToD RX flow

i2c read addr:0x62 offset :0x84(status) bit 1 → Check offset 0x84 bit0 is equal to 1 or not

i2c read addr:0x62 offset :0xB4(fifo.out) → Read data from fifo output data is ToD tx data

2.1.4.CPLD

CPLD locates on Main Board with connecting to CPU via I2C interface and I2C access address is 0x63.

The following features are available with the CPLD:

- FAN speed adjustment
- Fan detection
- SFP+ Port LED Link/Act indicates for Port 1 to Port 6
- SFP Port LED Link/Act indicates for Port 7 to Port 14
- SFP+ and SFP Port transceiver status detect (Mode Absent, Fault, Los, Disable.)
- I2C
- Reset

2.1.4.1. CPLD register

Address	Register	R/W	Default value
0x00	Board ID & COM TYPE	Read Only	
0x01	CPLD version	Read Only	
0x02	CPLD sub version	Read Only	
0x10	SFP+_PRESENT_Port01 ~08	Read Only	0xFF
0x11	SFP+_TX_Fault_Port 01 ~08	Read Only	0x00
0x12	SFP+_TX_Disable_Port 01 ~08	R/W	0x00
0x13	SFP+_RX_LOSS_Port01 ~08	Read Only	0x00
0x14	SFP+_PRESENT_Port09 ~17	Read Only	0xFF
0x15	SFP+_TX_Fault_Port09 ~17	Read Only	0x00
0x16	SFP+_TX_Disable_Port09 ~17	R/W	0x00
0x17	SFP+_RX_LOSS_Port09 ~17	Read Only	0x00
0x26	SFP+_Port1 LED	Read Only	0x03
0x27	SFP+_Port2 LED	Read Only	0x03
0x28	SFP+_Port3 LED	Read Only	0x03
0x29	SFP+_Port4 LED	Read Only	0x03
0x2A	SFP+_Port5 LED	Read Only	0x03
0x2B	SFP+_Port6 LED	Read Only	0x03
0x2C	SFP_Port7 LED	Read Only	0x03
0x2D	SFP_Port8 LED	Read Only	0x03
0x2E	SFP_Port9 LED	Read Only	0x03
0x2F	SFP_Port10 LED	Read Only	0x03
0x30	SFP_Port11 LED	Read Only	0x03
0x31	SFP_Port12 LED	Read Only	0x03
0x32	SFP_Port13 LED	Read Only	0x03
0x33	SFP_Port14 LED	Read Only	0x03
0x50	Reset	Read Only	0x01
0x60	LED_MODE	R/W	0x42
0x61	CPLD2_INT_Mode	R/W	0x00
0x70	SFP+_TXFLT_Port 1~8	R/W	0x00
0x71	SFP+_RXLOS_Port 1~8	R/W	0x00
0x72	SFP+_TXFLT_Port 9~16	R/W	0x00
0x73	SFP+_RXLOS_Port 9~16	R/W	0x00
0xA4	10G SFP+ Port1 LED	R/W	0xEF
0xA5	10G SFP+ Port2 LED	R/W	0xEF

Address	Register	R/W	Default value
0xA6	10G SFP+ Port3 LED	R/W	0xEF
0xA7	10G SFP+ Port4 LED	R/W	0xEF
0xA8	10G SFP+ Port5 LED	R/W	0xEF
0xA9	10G SFP+ Port6 LED	R/W	0xEF
0xAA	1G SFP Port7 LED	R/W	0xEF
0xAB	1G SFP Port8 LED	R/W	0xEF
0xAC	1G SFP Port9 LED	R/W	0xEF
0xAD	1G SFP Port10 LED	R/W	0xEF
0xAE	1G SFP Port11 LED	R/W	0xEF
0xAF	1G SFP Port12 LED	R/W	0xEF
0xB0	1G SFP Port13 LED	R/W	0xEF
0xB1	1G SFP Port14 LED	R/W	0xEF
0xBC	Blinking Speed	R/W	0x04
0xBD	Seven Segment LED	R/W	0x00
0xE0	Scratch Pad	R/W	0x00

Table 8 CPLD I/O Register Table

2.1.4.2. Offset 0x00 Board ID & COM TYPE (Read Only)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5	COM TYPE2	R		TBD
4	COM TYPE1	R		TBD
3	COM TYPE0	R		TBD
2	BOARD ID2	R		TBD
1	BOARD ID1	R		TBD
0	BOARD ID0	R		TBD

2.1.4.3. Offset 0x01 CPLD version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	CPLD version	R		CPLD version

2.1.4.4. Offset 0x02 CPLD sub version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	CPLD sub version	R		used for HW debug only

2.1.4.5. Offset 0x10 SFP+_PRESENT_Port01 ~08 (Read only)

Bit	Name	R/W	Reset Value	Description
7	MOD_ABS_08	R	1	0: indicates which SFP has been installed. 1: No SFP install
6	MOD_ABS_07	R	1	0: indicates which SFP has been installed. 1: No SFP install
5	MOD_ABS_06	R	1	0: indicates which SFP has been installed. 1: No SFP install
4	MOD_ABS_05	R	1	0: indicates which SFP has been installed. 1: No SFP install
3	MOD_ABS_04	R	1	0: indicates which SFP has been installed. 1: No SFP install
2	MOD_ABS_03	R	1	0: indicates which SFP has been installed. 1: No SFP install
1	MOD_ABS_02	R	1	0: indicates which SFP has been installed. 1: No SFP install
0	MOD_ABS_01	R	1	0: indicates which SFP has been installed. 1: No SFP install

2.1.4.6. Offset 0x11 SFP+_TX_Fault_Port 01 ~08 (Read only)

Bit	Name	R/W	Reset Value	Description
7	TXFLT_08	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
6	TXFLT_07	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
5	TXFLT_06	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault

4	TXFLT_05	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
3	TXFLT_04	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
2	TXFLT_03	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
1	TXFLT_02	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
0	TXFLT_01	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault

2.1.4.7. Offset 0x12 SFP+_TX_Disable_Port 01 ~08 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	TXDIS_08	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.
6	TXDIS_07	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.
5	TXDIS_06	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.
4	TXDIS_05	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.
3	TXDIS_04	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.
2	TXDIS_03	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.
1	TXDIS_02	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.
0	TXDIS_01	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.

2.1.4.8. Offset 0x13 SFP+_RX_LOSS_Port01 ~08 (Read only)

Bit	Name	R/W	Reset Value	Description
7	RXLOS_08	R	0	0: SFP+ optical level meet the standard 1: SFP+ optical level lower than the standard
6	RXLOS_07	R	0	0: SFP+ optical level meet the standard 1: SFP+ optical level lower than the standard
5	RXLOS_06	R	0	0: SFP+ optical level meet the standard 1: SFP+ optical level lower than the standard
4	RXLOS_05	R	0	0: SFP+ optical level meet the standard 1: SFP+ optical level lower than the standard
3	RXLOS_04	R	0	0: SFP+ optical level meet the standard 1: SFP+ optical level lower than the standard
2	RXLOS_03	R	0	0: SFP+ optical level meet the standard 1: SFP+ optical level lower than the standard
1	RXLOS_02	R	0	0: SFP+ optical level meet the standard 1: SFP+ optical level lower than the standard
0	RXLOS_01	R	0	0: SFP+ optical level meet the standard

				1: SFP+ optical level lower than the standard
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2.1.4.9. Offset 0x14 SFP+_PRESENT_Port09 ~14 (Read only)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5	MOD_ABS_14	R	1	0: indicates which SFP has been installed. 1: No SFP install
4	MOD_ABS_13	R	1	0: indicates which SFP has been installed. 1: No SFP install
3	MOD_ABS_12	R	1	0: indicates which SFP has been installed. 1: No SFP install
2	MOD_ABS_11	R	1	0: indicates which SFP has been installed. 1: No SFP install
1	MOD_ABS_10	R	1	0: indicates which SFP has been installed. 1: No SFP install
0	MOD_ABS_09	R	1	0: indicates which SFP has been installed. 1: No SFP install

2.1.4.10. Offset 0x15 SFP+_TX_Fault_Port09 ~14 (Read only)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5	TXFLT_14	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
4	TXFLT_13	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
3	TXFLT_12	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
2	TXFLT_11	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
1	TXFLT_10	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
0	TXFLT_09	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault

2.1.4.11. Offset 0x16 SFP+_TX_Disable_Port 09 ~14 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5	TXDIS_14	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.
4	TXDIS_13	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.
3	TXDIS_12	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.
2	TXDIS_11	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.
1	TXDIS_10	R/W	0	When a value of “1” is written, will turn off the

				laser's power for each SFP module.
0	TXDIS_09	R/W	0	When a value of "1" is written, will turn off the laser's power for each SFP module.

2.1.4.12. Offset 0x17 SFP+_RX_LOSS_Port 09 ~14 (Read only)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5	RXLOS_14	R	0	0: SFP+ optical level meet the standard 1: SFP+ optical level lower than the standard
4	RXLOS_13	R	0	0: SFP+ optical level meet the standard 1: SFP+ optical level lower than the standard
3	RXLOS_12	R	0	0: SFP+ optical level meet the standard 1: SFP+ optical level lower than the standard
2	RXLOS_11	R	0	0: SFP+ optical level meet the standard 1: SFP+ optical level lower than the standard
1	RXLOS_10	R	0	0: SFP+ optical level meet the standard 1: SFP+ optical level lower than the standard
0	RXLOS_09	R	0	0: SFP+ optical level meet the standard 1: SFP+ optical level lower than the standard

2.1.4.13. Offset 0x18 SFP+_RS (Read and Write)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5	SFP+_Port6_RS0	R/W	0	0: SFP+ Port6 operate at 1G 1: SFP+ Port6 operate at 10G
4	SFP+_Port5_RS0	R/W	0	0: SFP+ Port5 operate at 1G 1: SFP+ Port5 operate at 10G
3	SFP+_Port4_RS0	R/W	0	0: SFP+ Port4 operate at 1G 1: SFP+ Port4 operate at 10G
2	SFP+_Port3_RS0	R/W	0	0: SFP+ Port3 operate at 1G 1: SFP+ Port3 operate at 10G
1	SFP+_Port2_RS0	R/W	0	0: SFP+ Port2 operate at 1G 1: SFP+ Port2 operate at 10G
0	SFP+_Port1_RS0	R/W	0	0: SFP+ Port1 operate at 1G 1: SFP+ Port1 operate at 10G

2.1.4.14. Offset 0x26 SFP+_Port1 Configuration (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2	SFP+_P1_Speed1	R	0	01: 10G
1	SFP+_P1_Speed0	R	0	10: 1G
0	SFP+_P1_Link-up/Activity	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity

2.1.4.15. Offset 0x27 SFP+_Port2 Configuration (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2	SFP+_P2_Speed1	R	0	01: 10G 10: 1G
1	SFP+_P2_Speed0	R	0	
0	SFP+_P2_Link-up/Activity	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity

2.1.4.16. Offset 0x28 SFP+_Port3 Configuration (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2	SFP+_P3_Speed1	R	0	01: 10G 10: 1G
1	SFP+_P3_Speed0	R	0	
0	SFP+_P3_Link-up/Activity	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity

2.1.4.17. Offset 0x29 SFP+_Port4 Configuration (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2	SFP+_P4_Speed1	R	0	01: 10G 10: 1G
1	SFP+_P4_Speed0	R	0	
0	SFP+_P4_Link-up/Activity	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity

2.1.4.18. Offset 0x2A SFP+_Port5 Configuration (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2	SFP+_P5_Speed1	R	0	01: 10G 10: 1G
1	SFP+_P5_Speed0	R	0	
0	SFP+_P5_Link-up/Activity	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity

2.1.4.19. Offset 0x2B SFP+_Port6 Configuration (Read Only)

Bit	Name	R/W	Reset Value	Description
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7:3	(Reserved)	R/W	0	
2	SFP+_P6_Speed1	R	0	01: 10G
1	SFP+_P6_Speed0	R	0	10: 1G
0	SFP+_P6_Link-up/Activity	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity

2.1.4.20. Offset 0x2C SFP_Port7 Configuration (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2	SFP_P7_Speed1	R	0	01: 1G
1	SFP_P7_Speed0	R	0	10: 2.5G
0	SFP_P7_Link-up/Activity	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity

2.1.4.21. Offset 0x2D SFP_Port8 Configuration (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2	SFP_P8_Speed1	R	0	01: 1G
1	SFP_P8_Speed0	R	0	10: 2.5G
0	SFP_P8_Link-up/Activity	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity

2.1.4.22. Offset 0x2E SFP_Port9 Configuration (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2	SFP_P9_Speed1	R	0	01: 1G
1	SFP_P9_Speed0	R	0	10: 2.5G
0	SFP_P9_Link-up/Activity	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity

2.1.4.23. Offset 0x2F SFP_Port10 Configuration (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2	SFP_P10_Speed1	R	0	01: 1G

1	SFP_P10_Speed0	R	0	10: 2.5G
0	SFP_P10_Link-up/Activity	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity

2.1.4.24. Offset 0x30 SFP_Port11 Configuration (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2	SFP_P11_Speed1	R	0	01: 1G
1	SFP_P11_Speed0	R	0	10: 2.5G
0	SFP_P11_Link-up/Activity	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity

2.1.4.25. Offset 0x31 SFP_Port12 Configuration (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2	SFP_P12_Speed1	R	0	01: 1G
1	SFP_P12_Speed0	R	0	10: 2.5G
0	SFP_P12_Link-up/Activity	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity

2.1.4.26. Offset 0x32 SFP_Port13 Configuration (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2	SFP_P13_Speed1	R	0	01: 1G
1	SFP_P13_Speed0	R	0	10: 2.5G
0	SFP_P13_Link-up/Activity	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity

2.1.4.27. Offset 0x33 SFP_Port14 Configuration (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2	SFP_P14_Speed1	R	0	01: 1G
1	SFP_P14_Speed0	R	0	10: 2.5G
0	SFP_P14_Link-up/Activity	R	0	0: The Led light is off. 1: The Led light is on.

				Toggle: Activity
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2.1.4.28. Offset 0x50 Reset(Read& Write)

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2	CPLD_RST	R		
1	FPGA_SPI_RST_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
0	ZL30773 I2C SPI CS	R/W	1	

2.1.4.29. Offset 0x60 LED Control Register (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	Reserved			
6:4	LED Mode	R/W	100	000: AUTO Polling (Amber =>Green cycle) 001: LED Test Mode (bit[2:0]) 010: LED Stream mode 011: LED CPU control Mode 100: LED control by CPU and LED stream separately.
3	LED Blinking	R/W	0	This bit is valid when LED Mode=000 or 001. 0: No Blinking 1: Blinking
2	SFP_LED_A	R/W	0	LED_AMBER 0: LED_RED is ON 1: LED_RED is OFF
1	SFP_LED_G	R/W	1	LED_GREEN 0: LED_GREEN is ON 1: LED_GREEN is OFF
0	Reserved			

2.1.4.30. Offset 0x61 CPLD2_INT_Mode (Read& Write)

Bit	Name	R/W	Reset Value	Description
1	CPLD2_INT	R/W	0	When Test mode enable 0: CPLD2_INT output is low. 1: CPLD2_INT output is high
0	CPLD2_INT_Mode	R/W	0	0: Normal mode 1: Test Mode

2.1.4.31. Offset 0x62 CPLD2 INT Flag (Read & Write)

Bit	Name	R/W	Reset Value	Description
2	TXFLT_IF	R/W	0	0: All SFP Module TXFLT status have no change. 1: When TXFLT_x mask is 0 , x of SFP modules's TXFLT toggle will set this flag.

				When enter PCIE msi interrupt subroutine. User should clear this flag by write 1 to this bit for clear state.
1	RXLOS_IF	R/W	0	0: All SFP Module RXLOS status have no change. 1: When RXLOS_x mask is 0 , x of SFP modules's RXLOS toggle will set this flag. When enter PCIE msi interrupt subroutine. User has to clear this flag by write 1 to this bit for clear state.
0	MOD_ABS_IF	R/W	0	0:All SFP module MOD ABS status have no change. 1: When MOD_ABS_x_mask is 0, x of SFP modules installed or uninstalled will set this flag. When enter PCIE msi interrupt subroutine. User has to clear this flag by write 1 to this bit for clear state.

2.1.4.32. Offset 0x64 SFP+_MOD_ABS_Mask_Port 1~8 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	MOD_ABS_8_Mask	R/W	1	1: MOD_ABS_8 Interrupt function disable 0: MOD_ABS_8 Interrupt function enable
6	MOD_ABS_7_Mask	R/W	1	1: MOD_ABS_7 Interrupt function disable 0: MOD_ABS_7 Interrupt function enable
5	MOD_ABS_6_Mask	R/W	1	1: MOD_ABS_6 Interrupt function disable 0: MOD_ABS_6 Interrupt function enable
4	MOD_ABS_5_Mask	R/W	1	1: MOD_ABS_5 Interrupt function disable 0: MOD_ABS_5 Interrupt function enable
3	MOD_ABS_4_Mask	R/W	1	1: MOD_ABS_4 Interrupt function disable 0: MOD_ABS_4 Interrupt function enable
2	MOD_ABS_3_Mask	R/W	1	1: MOD_ABS_3 Interrupt function disable 0: MOD_ABS_3 Interrupt function enable
1	MOD_ABS_2_Mask	R/W	1	1: MOD_ABS_2 Interrupt function disable 0: MOD_ABS_2 Interrupt function enable
0	MOD_ABS_1_Mask	R/W	1	1: MOD_ABS_1 Interrupt function disable 0: MOD_ABS_1 Interrupt function enable

2.1.4.33. Offset 0x65 SFP+_MOD_ABS_Mask_Port 9~14 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5	MOD_ABS_14_Mask	R/W	1	1: MOD_ABS_14 Interrupt function disable 0: MOD_ABS_14 Interrupt function enable
4	MOD_ABS_13_Mask	R/W	1	1: MOD_ABS_13 Interrupt function disable 0: MOD_ABS_13 Interrupt function enable
3	MOD_ABS_12_Mask	R/W	1	1: MOD_ABS_12 Interrupt function disable 0: MOD_ABS_12 Interrupt function enable

2	MOD_ABS_11_Mask	R/W	1	1: MOD_ABS_11 Interrupt function disable 0: MOD_ABS_11 Interrupt function enable
1	MOD_ABS_10_Mask	R/W	1	1: MOD_ABS_10 Interrupt function disable 0: MOD_ABS_10 Interrupt function enable
0	MOD_ABS_9_Mask	R/W	1	1: MOD_ABS_9 Interrupt function disable 0: MOD_ABS_9 Interrupt function enable

2.1.4.34. Offset 0x70 SFP+_TXFLT_Mask_Port 1~8 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	TXFLT8_Mask	R/W	0	1: TXFLT_8 Interrupt function disable 0: TXFLT_8 Interrupt function enable
6	TXFLT7_Mask	R/W	0	1: TXFLT_7 Interrupt function disable 0: TXFLT_7 Interrupt function enable
5	TXFLT6_Mask	R/W	0	1: TXFLT_6 Interrupt function disable 0: TXFLT_6 Interrupt function enable
4	TXFLT5_Mask	R/W	0	1: TXFLT_5 Interrupt function disable 0: TXFLT_5 Interrupt function enable
3	TXFLT4_Mask	R/W	0	1: TXFLT_4 Interrupt function disable 0: TXFLT_4 Interrupt function enable
2	TXFLT3_Mask	R/W	0	1: TXFLT_3 Interrupt function disable 0: TXFLT_3 Interrupt function enable
1	TXFLT2_Mask	R/W	0	1: TXFLT_2 Interrupt function disable 0: TXFLT_2 Interrupt function enable
0	TXFLT1_Mask	R/W	0	1: TXFLT_1 Interrupt function disable 0: TXFLT_1 Interrupt function enable

2.1.4.35. Offset 0x71 SFP+_RXLOS_Mask_Port 1~8 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	RXLOS8_Mask	R/W	0	1: RXLOS_8 Interrupt function disable 0: RXLOS_8 Interrupt function enable
6	RXLOS7_Mask	R/W	0	1: RXLOS_7 Interrupt function disable 0: RXLOS_7 Interrupt function enable
5	RXLOS6_Mask	R/W	0	1: RXLOS_6 Interrupt function disable 0: RXLOS_6 Interrupt function enable
4	RXLOS5_Mask	R/W	0	1: RXLOS_5 Interrupt function disable 0: RXLOS_5 Interrupt function enable
3	RXLOS4_Mask	R/W	0	1: RXLOS_4 Interrupt function disable 0: RXLOS_4 Interrupt function enable
2	RXLOS3_Mask	R/W	0	1: RXLOS_3 Interrupt function disable 0: RXLOS_3 Interrupt function enable
1	RXLOS2_Mask	R/W	0	1: RXLOS_2 Interrupt function disable 0: RXLOS_2 Interrupt function enable
0	RXLOS1_Mask	R/W	0	1: RXLOS_1 Interrupt function disable 0: RXLOS_1 Interrupt function enable

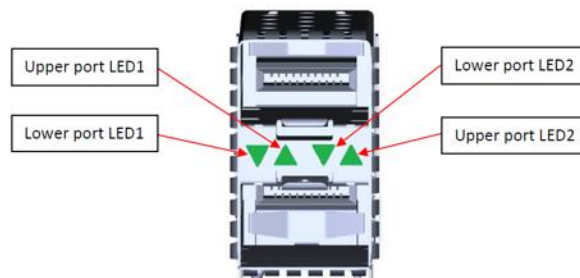
2.1.4.36. Offset 0x72 SFP+_TXFLT_Mask_Port 9~14 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5	TXFLT14_Mask	R/W	0	1: TXFLT_14 Interrupt function disable 0: TXFLT_14 Interrupt function enable
4	TXFLT13_Mask	R/W	0	1: TXFLT_13 Interrupt function disable 0: TXFLT_13 Interrupt function enable
3	TXFLT12_Mask	R/W	0	1: TXFLT_12 Interrupt function disable 0: TXFLT_12 Interrupt function enable
2	TXFLT11_Mask	R/W	0	1: TXFLT_11 Interrupt function disable 0: TXFLT_11 Interrupt function enable
1	TXFLT10_Mask	R/W	0	1: TXFLT_10 Interrupt function disable 0: TXFLT_10 Interrupt function enable
0	TXFLT9_Mask	R/W	0	1: TXFLT_9 Interrupt function disable 0: TXFLT_9 Interrupt function enable

2.1.4.37. Offset 0x73 SFP+_RXLOS_Mask_Port 9~14 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5	RXLOS14_Mask	R/W	0	1: RXLOS_14 Interrupt function disable 0: RXLOS_14 Interrupt function enable
4	RXLOS13_Mask	R/W	0	1: RXLOS_13 Interrupt function disable 0: RXLOS_13 Interrupt function enable
3	RXLOS12_Mask	R/W	0	1: RXLOS_12 Interrupt function disable 0: RXLOS_12 Interrupt function enable
2	RXLOS11_Mask	R/W	0	1: RXLOS_11 Interrupt function disable 0: RXLOS_11 Interrupt function enable
1	RXLOS10_Mask	R/W	0	1: RXLOS_10 Interrupt function disable 0: RXLOS_10 Interrupt function enable
0	RXLOS9_Mask	R/W	0	1: RXLOS_9 Interrupt function disable 0: RXLOS_9 Interrupt function enable

2.1.4.38. Offset 0xA4 10G SFP+ Port1 LED (Read& Write)



Bit	Name	R/W	Reset Value	Description
7:5	Reserved			

4	LED2 Green	R/W	0	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
3	LED2 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
2	LED1 Green	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
1	LED1 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
0	Blinking for LED2	R/W	1	This bit is valid when LED Mode=011 1: Blinking 0: Unblinking

2.1.4.39. Offset 0xA5 10G SFP+ Port2 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved			
4	LED2 Green	R/W	0	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
3	LED2 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
2	LED1 Green	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
1	LED1 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
0	Blinking for LED2	R/W	1	This bit is valid when LED Mode=011 1: Blinking 0: Unblinking

2.1.4.40. Offset 0xA6 10G SFP+ Port3 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved			
4	LED2 Green	R/W	0	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
3	LED2 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
2	LED1 Green	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON

1	LED1 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
0	Blinking for LED2	R/W	1	This bit is valid when LED Mode=011 1: Blinking 0: Unblinking

2.1.4.41. Offset 0xA7 10G SFP+ Port4 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved			
4	LED2 Green	R/W	0	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
3	LED2 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
2	LED1 Green	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
1	LED1 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
0	Blinking for LED2	R/W	1	This bit is valid when LED Mode=011 1: Blinking 0: Unblinking

2.1.4.42. Offset 0xA8 10G SFP+ Port5 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved			
4	LED2 Green	R/W	0	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
3	LED2 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
2	LED1 Green	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
1	LED1 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
0	Blinking for LED2	R/W	1	This bit is valid when LED Mode=011 1: Blinking 0: Unblinking

2.1.4.43. Offset 0xA9 10G SFP+ Port6 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved			
4	LED2 Green	R/W	0	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
3	LED2 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
2	LED1 Green	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
1	LED1 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
0	Blinking for LED2	R/W	1	This bit is valid when LED Mode=011 1: Blinking 0: Unblinking

2.1.4.44. Offset 0xAA 1G SFP Port7 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved			
4	LED2 Green	R/W	0	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
3	LED2 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
2	LED1 Green	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
1	LED1 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
0	Blinking for LED2	R/W	1	This bit is valid when LED Mode=011 1: Blinking 0: Unblinking

2.1.4.45. Offset 0xAB 1G SFP Port8 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved			
4	LED2 Green	R/W	0	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
3	LED2 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON

2	LED1 Green	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
1	LED1 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
0	Blinking for LED2	R/W	1	This bit is valid when LED Mode=011 1: Blinking 0: Unblinking

2.1.4.46. Offset 0xAC 1G SFP+ Port9 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved			
4	LED2 Green	R/W	0	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
3	LED2 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
2	LED1 Green	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
1	LED1 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
0	Blinking for LED2	R/W	1	This bit is valid when LED Mode=011 1: Blinking 0: Unblinking

2.1.4.47. Offset 0xAD 1G SFP Port10 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved			
4	LED2 Green	R/W	0	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
3	LED2 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
2	LED1 Green	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
1	LED1 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
0	Blanking for LED2	R/W	1	This bit is valid when LED Mode=011 1: Blinking 0: Unblinking

2.1.4.48. Offset 0xAE 1G SFP Port11 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved			
4	LED2 Green	R/W	0	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
3	LED2 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
2	LED1 Green	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
1	LED1 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
0	Blinking for LED2	R/W	1	This bit is valid when LED Mode=011 1: Blinking 0: Unblinking

2.1.4.49. Offset 0xAF 1G SFP Port12 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved			
4	LED2 Green	R/W	0	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
3	LED2 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
2	LED1 Green	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
1	LED1 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
0	Blinking for LED2	R/W	1	This bit is valid when LED Mode=011 1: Blinking 0: Unblinking

2.1.4.50. Offset 0xB0 1G SFP Port13 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved			
4	LED2 Green	R/W	0	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
3	LED2 Amber	R/W	1	This bit is valid when LED Mode=011 or 100

				1: LED OFF 0: LED ON
2	LED1 Green	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
1	LED1 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
0	Blinking for LED2	R/W	1	This bit is valid when LED Mode=011 1: Blinking 0: Unblinking

2.1.4.51. Offset 0xB1 1G SFP Port14 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved			
4	LED2 Green	R/W	0	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
3	LED2 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
2	LED1 Green	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
1	LED1 Amber	R/W	1	This bit is valid when LED Mode=011 or 100 1: LED OFF 0: LED ON
0	Blinking for LED2	R/W	1	This bit is valid when LED Mode=011 1: Blinking 0: Unblinking

2.1.4.52. Offset 0xBC Blinking Speed (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			
3	Blinking Speed	R/W	0100	0000: 20.48ms 0001: 40.96ms 0010: 81.92ms 0011: 163.84ms 0100: 327.68ms 0101: 655.36ms 0110: 1310.72ms

2.1.4.53. Offset 0xBD Seven Segment LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			

3:0	Seven Segment LED	R/W	0000	0000: show 0 in seven segment led 0001: show 1 in seven segment led 0010: show 2 in seven segment led 0011: show 3 in seven segment led 0100: show 4 in seven segment led 0101: show 5 in seven segment led 0110: show 6 in seven segment led 0111: show 7 in seven segment led 1000: show 8 in seven segment led 1001: show 9 in seven segment led 1010~1110: no display 1111: dot
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2.1.4.54. Offset 0xE0 Scratch_Pad (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	Scratch Pad	R/W	0x00	This for SW R/W test

2.1.5.Fan Part in the CPLD

The following features are available with the CPLD:

- FAN speed adjustment
- Fan detection
- Reset

The CPU can access FAN CPLD via I2C interface to get the fan status.

The Fan CPLD has the register to control Fan PWM signal for fan speed control, and the counter for fan speed reporting. There is a fan power control to enable/ disable Fan power rail.

The CPLD will detect fan speed to check fan status if there is any issue. And CPLD will inform CPU by fan interrupt signal if there has fan fail occur, temp sensor alert or watchdog time out.

Fan Control

Front fan max speed is 13400RPM, and rear fan max speed is 13700RPM.Period time is 200ms, CPLD counts negative waveform and records it at 0x20~0x23.

$$200\text{ms} / T \text{ ms} = m \text{ (times / sec)}$$

$$200\text{ms} / (1/2 * TS) = m \text{ (times / sec)}$$

$$200\text{ms}/m \text{ (times / sec)}= 1/2 * TS$$

$$TS = 60/N$$

$$N=60/TS= 60/0.4*m=150*m \text{ (times / sec)}$$

SW must multiple 150 and show it as RPM(Revolutions per minute).

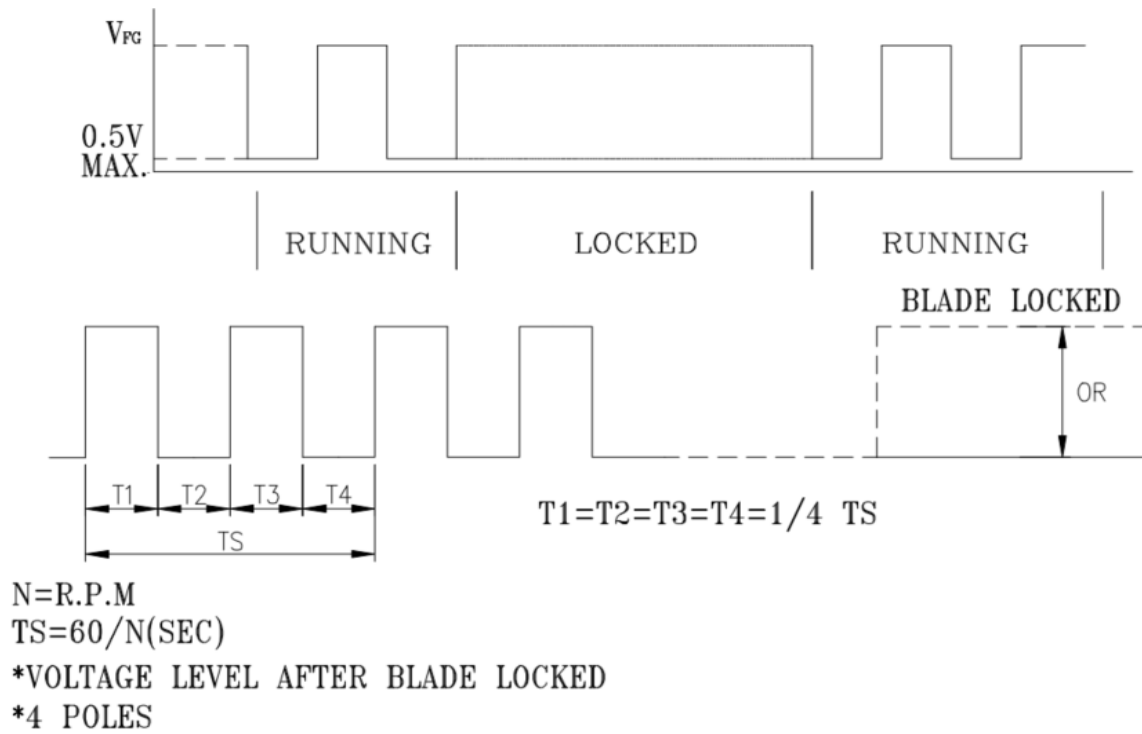


Figure 4 Fan Tachometer Output Waveform

Fan PWM set duty cycle table shown in below table

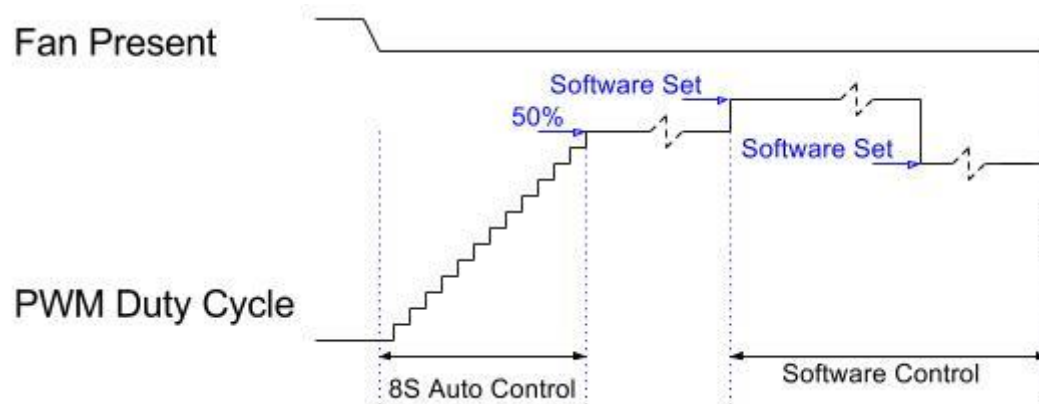
Table 9 – FAN PWM Setting

FAN_PWM[5:0]	
00 0000	0/63 or 0% duty cycle
00 0001	1/63 or 1.549% duty cycle
00 0010	2/63 or 3.116% duty cycle
00 0011	3/63 or 4.671 % duty cycle
00 0100	4/63 or 6.235% duty cycle
00 0101	5/63 or 7.804% duty cycle
00 0110	6/63 or 9.358% duty cycle
00 0111	7/63 or 10.923 % duty cycle
00 1000	8/63 or 12.485 % duty cycle
00 1001	9/63 or 14.047 % duty cycle
00 1010	10/63 or 15.611 % duty cycle
00 1011	11/63 or 17.174 % duty cycle
00 1100	12/63 or 18.732 % duty cycle
00 1101	13/63 or 20.295 % duty cycle
00 1110	14/63 or 21.864 % duty cycle
00 1111	15/63 or 23.414 % duty cycle
01 0000	16/63 or 24.987 % duty cycle
01 0001	17/63 or 26.553 % duty cycle
01 0010	18/63 or 28.121 % duty cycle
01 0011	19/63 or 29.678 % duty cycle
01 0100	20/63 or 31.234 % duty cycle
01 0101	21/63 or 32.795 % duty cycle
01 0110	22/63 or 34.375 % duty cycle
01 0111	23/63 or 35.923 % duty cycle
01 1000	24/63 or 37.482 % duty cycle
01 1001	25/63 or 39.048 % duty cycle
01 1010	26/63 or 40.617 % duty cycle
01 1011	27/63 or 42.177 % duty cycle
01 1100	28/63 or 43.732 % duty cycle
01 1101	29/63 or 45.303 % duty cycle
01 1110	30/63 or 46.863 % duty cycle
01 1111	31/63 or 49.900 % duty cycle
10 0000	32/63 or 51.546 % duty cycle
10 0001	33/63 or 53.109 % duty cycle
10 0010	34/63 or 54.669 % duty cycle
10 0011	35/63 or 56.234 % duty cycle
10 0100	36/63 or 57.789 % duty cycle
10 0101	37/63 or 59.369 % duty cycle
10 0110	38/63 or 60.932 % duty cycle
10 0111	39/63 or 62.495 % duty cycle

10_1000	40/63 or 64.041 % duty cycle
10_1001	41/63 or 65.613 % duty cycle
10_1010	42/63 or 67.177 % duty cycle
10_1011	43/63 or 68.745 % duty cycle
10_1100	44/63 or 70.295 % duty cycle
10_1101	45/63 or 71.863 % duty cycle
10_1110	46/63 or 73.419 % duty cycle
10_1111	47/63 or 74.975 % duty cycle
11_0000	48/63 or 76.553 % duty cycle
11_0001	49/63 or 78.106 % duty cycle
11_0010	50/63 or 79.671 % duty cycle
11_0011	51/63 or 81.234 % duty cycle
11_0100	52/63 or 82.796 % duty cycle
11_0101	53/63 or 84.349 % duty cycle
11_0110	54/63 or 85.925 % duty cycle
11_0111	55/63 or 87.482 % duty cycle
11_1000	56/63 or 89.039 % duty cycle
11_1001	57/63 or 90.606 % duty cycle
11_1010	58/63 or 92.169 % duty cycle
11_1011	59/63 or 93.736 % duty cycle
11_1100	60/63 or 95.297 % duty cycle
11_1101	61/63 or 96.861 % duty cycle
11_1110	62/63 or 98.424 % duty cycle
11_1111	63/63 or 100.00 % duty cycle

In order to reduce the inrush current after Fan present, CPLD will auto control the Fan PWM value after Fan presented. By default the Fan PWM target value will set to 50%. CPLD will take 8S to increase the PWM duty cycle from 0% to 50%. Every 500mS increase a duty cycle level.

Below figure shows out the Fan present status and the PWM Duty Cycle output status.



2.1.5.1. CPLD register

Address	Register	R/W	Default value
0x00	BOARD VERSION	Read Only	
0x01	CPLD version	Read Only	
0x02	CPLD SUB VERSION	Read Only	
0x08	FAN INT TRIG MOD	Read& Write	
0x09	FAN INT RPT	Read Only	
0x0A	FAN WDT TRIGGER	Read& Write	
0x0B	FAN WDT DIVIDER CLOCK	Read& Write	
0x0C	FAN READ WDT COUNTER	Read Only	
0x0D	FAN CLK DIVIDER TECK	Read& Write	
0x0E	FAN CLK DIVIDER PWM	Read& Write	
0x10	FAN_ENABLE_REG	Read& Write	
0x20	FAN1 TACH	Read Only	
0x21	FAN1 PWM	Read& Write	
0x22	FAN1 PRESENT	Read Only	
0x23	FAN1 INT MASK	Read& Write	
0x24	FAN1 INT STA	Read Only	
0x30	FAN2 TACH	Read Only	
0x31	FAN2 PWM	Read& Write	
0x32	FAN2 PRESENT	Read Only	
0x33	FAN2 INT MASK	Read& Write	
0x34	FAN2 INT STA	Read Only	
0x40	FAN3 TACH	Read Only	
0x41	FAN3 PWM	Read& Write	
0x42	FAN3 PRESENT	Read Only	
0x43	FAN3 INT MASK	Read& Write	
0x44	FAN3 INT STA	Read Only	
0x50	FAN4 TACH	Read Only	
0x51	FAN4 PWM	Read& Write	
0x52	FAN4 PRESENT	Read Only	
0x53	FAN4 INT MASK	Read& Write	
0x54	FAN4 INT STA	Read Only	
~~0x60~~	~~FAN5 TACH~~	~~Read Only~~	
~~0x61~~	~~FAN5 PWM~~	~~Read& Write~~	
~~0x62~~	~~FAN5 PRESENT~~	~~Read Only~~	
~~0x63~~	~~FAN5 INT MASK~~	~~Read& Write~~	
~~0x64~~	~~FAN5 INT STA~~	~~Read Only~~	
0x70	ALARM	Read Only	
0x78	ALARM MASK	Read& Write	

Table 10 Fan CPLD I/O Register Table

2.1.5.1.1 Offset 0x00 BOARD_VERSION (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:4]	Reserved	R		Reserved
[3:2]	Version_ID	R		
[1:0]	Board_ID	R		

2.1.5.1.2 Offset 0x01 CPLD Version (Read Only)

Bit	Name	R/W	Reset Value	Description
[7]	Reserved	R		Reserved
[6]	Released Bit	R		0= not released 1= Released version after PVT
[5:0]	CPLD_ver[5:0]	R		CPLD version

2.1.5.1.3 Offset 0x02 CPLD_SUB_VERSION (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:0]	CPLD_SUB_VERSION	R		CPLD sub-version, used for HW debug only

2.1.5.1.4 Offset 0x08 FAN_INT_TRIG_MOD(Read& Write)

Bit	Name	R/W	Reset Value	Description
[7:2]	Reserved			
[1:0]	FAN_INT_TRIG			00: FAN interrupt trigger by falling edge 01: FAN interrupt trigger by rising edge 10: FAN interrupt trigger by both falling edge and rising edge 11: FAN interrupt trigger by low level

2.1.5.1.5 Offset 0x09 FAN_INT_RPT (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:5]	Reserved	N/A	N/A	Reserved
[4]	FAN5_INT	R		FanTray-5 Interrupt 0: No interrupt 1: Fan5 interrupt is active
[3]	FAN4_INT	R		FanTray-4 Interrupt 0: No interrupt 1: Fan4 interrupt is active
[2]	FAN3_INT	R		FanTray-3 Interrupt 0: No interrupt 1: Fan3 interrupt is active
[1]	FAN2_INT	R		FanTray-2 Interrupt 0: No interrupt 1: Fan2 interrupt is active
[0]	FAN1_INT	R		FanTray-1 Interrupt 0: No interrupt 1: Fan1 interrupt is active

2.1.5.1.6 Offset 0x0A BMC_WDT_TRIGGER (Read& Write)

Bit	Name	R/W	Reset Value	Description
[7:1]	Reserved	RO		Reserved
[0]	BMC_WDT_TRIGGER	R/W		0: Enable watchdog 1: Disable watchdog

2.1.5.1.7 Offset 0x0B FAN_WDT_DIVIDER_CLOCK (Read& Write)

Bit	Name	R/W	Reset Value	Description
[7:6]	FAN_WDT_DIVIDER_CLOCK	R/W	01	
[5:0]	FAN_SET_WDT_COUNTER	R/W	110001	

FAN_SET_WDT_COUNTER_REG[7:6]	Watchdog clock
00	0.67s
01	1.34s
10	2.68s
11	5.37s

Watchdog timer = Divider clock * counter

Ex. Divider clock = 2'b01 → 1.34

Counter = 6'b110001 → 49

Watchdog timer = 1.34 * 49 = 65.66 sec

2.1.5.1.8 Offset 0x0C FAN_READ_WDT_COUNTER (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:6]	Reserved			
[5:0]	FAN_READ_WDT_COUNTER	RO		

2.1.5.1.9 Offset 0x0D FAN_CLK_DIVIDER_TECK (Read & Write)

Bit	Name	R/W	Reset Value	Description
[7:6]	CLK_DIVIDER_TECK	R/W	01	Refer to below table.
[5:0]	TECK_COUNTER	R/W	001000	

CLK_DIVIDER_TECK_REG[7:6]	tachometer sample timer
00	10.48ms
01	20.97ms
10	41.94ms
11	83.89ms

Teck speed timer = CLK_DIVIDER_TECK * counter

Ex. CLK_DIVIDER_TECK = 2'b01 → 20.97ms

Counter = 6'b001000 → 8

Teck speed timer = 20.97ms * 8 = 167.76 ms

2.1.5.1.10 Offset 0x0E FAN_CLK_DIVIDER_PWM (Read & Write)

Bit	Name	R/W	Reset Value	Description
[7:4]	Reserved	N/A	N/A	Reserved
[2:0]	CLK_DIVIDER_PWM_REG	R/W	010	

CLK_DIVIDER_PWM_REG [2:0]	tachometer sample frequency (Hz)
000	6.25MHz
001	3.125MHz
010	1.5625MHz
011	781.25K
100	390.63K
101	195.31K
110	97.66K
111	48.83K

2.1.5.1.11 Offset 0x10 FAN_ENABLE_REG (Read & Write)

Bit	Name	R/W	Reset Value	Description
[7:5]	Reserved	N/A	N/A	Reserved
[4]	FAN5_ENABLE_REG	R/W	1	FAN5 Power Supply Enable 1: Enable the fan Power 0: Disable the fan power
[3]	FAN4_ENABLE_REG	R/W	1	FAN4 Power Supply Enable 1: Enable the fan Power 0: Disable the fan power
[2]	FAN3_ENABLE_REG	R/W	1	FAN3 Power Supply Enable 1: Enable the fan Power 0: Disable the fan power
[1]	FAN2_ENABLE_REG	R/W	1	FAN2 Power Supply Enable 1: Enable the fan Power 0: Disable the fan power
[0]	FAN1_ENABLE_REG	R/W	1	FAN1 Power Supply Enable 1: Enable the fan Power 0: Disable the fan power

2.1.5.1.12 Offset 0x20 FAN1_TACH (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:0]	FAN1_TACH_F_N	RO		Fan1 Fan Speed

2.1.5.1.13 Offset 0x21 FAN1_PWM (Read& Write)

Bit	Name	R/W	Reset Value	Description
[7:6]	Reserved			
[5:0]	FAN1_PWM	R/W		FAN1_PWM[7:0] FanTray-1 PWM control signal Please refer to Table3 for the mapping to fan duty cycle.

2.1.5.1.14 Offset 0x22 FAN1_PRESENT (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:2]	Reserved	RO		Reserved
[1]	FAN1_ALIVE	RO		Fan1 Alive Status 0: alive 1: bad
[0]	FAN1_PRESENT	RO		FanTray-1 Present 0: present 1: not present

2.1.5.1.15 Offset 0x23 FAN1_INT_MASK (Read& Write)

Bit	Name	R/W	Reset Value	Description
[7:2]	Reserved			Reserved
[1]	FAN1_ALIVE_MASK	R/W	1	Fan1 Alive Status Interrupt Mask 0: not mask 1: mask
[0]	FAN1_PRE_MASK	R/W	1	FanTray-1 Present Interrupt Mask 0: not mask 1: mask

2.1.5.1.16 Offset 0x24 FAN1_INT_STA (Read& Write)

Bit	Name	R/W	Reset Value	Description
[7:2]	Reserved	R/W		Reserved
[1]	FAN1_ALIVE_STA	WC		Fan1 Alive Status Interrupt Status 0: not interrupt 1: interrupt happened
[0]	FAN1_PRE_STA	WC		FanTray-1 Present Interrupt Status 0: not interrupt 1: interrupt happened

2.1.5.1.17 Offset 0x30 FAN2_TACH (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:0]	FAN2_TACH_F_N	RO		Fan2 Fan Speed

2.1.5.1.18 Offset 0x31 FAN2_PWM (Read& Write)

Bit	Name	R/W	Reset Value	Description
[7:6]	Reserved			
[5:0]	FAN2_PWM	R/W		FAN2_PWM[7:0] FanTray-2 PWM control signal Please refer to Table3 for the mapping to fan duty cycle.

2.1.5.1.19 Offset 0x32 FAN2_PRESENT (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:2]	Reserved	RO		Reserved
[1]	FAN2_ALIVE	RO		Fan2 Alive Status 0: alive

				1: bad
[0]	FAN2_PRESENT	RO		FanTray-2 Present 0: present 1: not present

2.1.5.1.20 Offset 0x33 FAN2_INT_MASK (Read& Write)

Bit	Name	R/W	Reset Value	Description
[7:2]	Reserved			Reserved
[1]	FAN2_ALIVE_MASK	R/W	1	Fan2 Alive Status Interrupt Mask 0: not mask 1: mask
[0]	FAN2_PRE_MASK	R/W	1	FanTray-2 Present Interrupt Mask 0: not mask 1: mask

2.1.5.1.21 Offset 0x34 FAN2_INT_STA (Read& Write)

Bit	Name	R/W	Reset Value	Description
[7:2]	Reserved	R/W		Reserved
[1]	FAN2_ALIVE_STA	WC		Fan2 Alive Status Interrupt Status 0: not interrupt 1: interrupt happened
[0]	FAN2_PRE_STA	WC		FanTray-2 Present Interrupt Status 0: not interrupt 1: interrupt happened

2.1.5.1.22 Offset 0x40 FAN3_TACH (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:0]	FAN3_TACH_F_N	RO		Fan3 Fan Speed

2.1.5.1.23 Offset 0x41 FAN3_PWM (Read& Write)

Bit	Name	R/W	Reset Value	Description
[7:6]	Reserved			
[5:0]	FAN3_PWM	R/W		FAN3_PWM[7:0] FanTray-3 PWM control signal Please refer to Table3 for the mapping to fan duty cycle.

2.1.5.1.24 Offset 0x42 FAN3_PRESENT (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:2]	Reserved	RO		Reserved
[1]	FAN3_ALIVE	RO		Fan3Alive Status 0: alive 1: bad
[0]	FAN3_PRESENT	RO		FanTray-3 Present 0: present 1: not present

2.1.5.1.25 Offset 0x43 FAN3_INT_MASK (Read& Write)

Bit	Name	R/W	Reset Value	Description
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[7:2]	Reserved			Reserved
[1]	FAN3_ALIVE_MASK	R/W	1	Fan3 Alive Status Interrupt Mask 0: not mask 1: mask
[0]	FAN3_PRE_MASK	R/W	1	FanTray-3 Present Interrupt Mask 0: not mask 1: mask

2.1.5.1.26 Offset 0x44 FAN3_INT_STA (Read& Write)

Bit	Name	R/W	Reset Value	Description
[7:2]	Reserved	R/W		Reserved
[1]	FAN3_ALIVE_STA	WC		Fan3 Alive Status Interrupt Status 0: not interrupt 1: interrupt happened
[0]	FAN3_PRE_STA	WC		FanTray-3 Present Interrupt Status 0: not interrupt 1: interrupt happened

2.1.5.1.27 Offset 0x50 FAN4_TACH (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:0]	FAN4_TACH_F_N	RO		Fan4 Fan Speed

2.1.5.1.28 Offset 0x51 FAN4_PWM (Read& Write)

Bit	Name	R/W	Reset Value	Description
[7:6]	Reserved			
[5:0]	FAN4_PWM	R/W		FAN4_PWM[7:0] FanTray-4 PWM control signal Please refer to Table3 for the mapping to fan duty cycle.

2.1.5.1.29 Offset 0x52 FAN4_PRESENT (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:2]	Reserved	RO		Reserved
[1]	FAN4_ALIVE	RO		Fan4 Alive Status 0: alive 1: bad
[0]	FAN4_PRESENT	RO		FanTray-4 Present 0: present 1: not present

2.1.5.1.30 Offset 0x53 FAN4_INT_MASK (Read& Write)

Bit	Name	R/W	Reset Value	Description
[7:2]	Reserved			Reserved
[1]	FAN4_ALIVE_MASK	R/W	1	Fan4 Alive Status Interrupt Mask 0: not mask 1: mask
[0]	FAN4_PRE_MASK	R/W	1	FanTray-4 Present Interrupt Mask 0: not mask 1: mask

2.1.5.1.31 Offset 0x54 FAN4_INT_STA (Read& Write)

Bit	Name	R/W	Reset Value	Description
[7:2]	Reserved	R/W		Reserved
[1]	FAN4_ALIVE_STA	WC		Fan4 Alive Status Interrupt Status 0: not interrupt 1: interrupt happened
[0]	FAN4_PRE_STA	WC		FanTray-4 Present Interrupt Status 0: not interrupt 1: interrupt happened

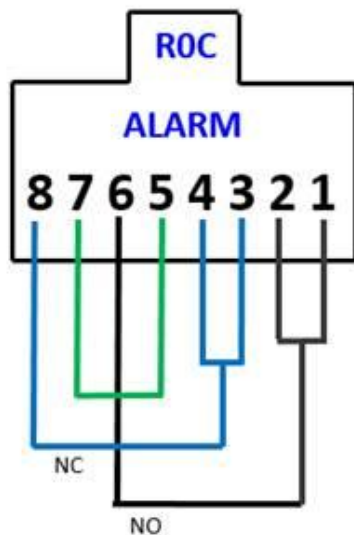
2.1.5.1.32 Offset 0x70 ALARM (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:4]	Reserved	R/W		Reserved
[3]	ALARM3	R		Alarm3 from fan board RJ45 0: interrupt happened 1: not interrupt
[2]	ALARM2	R		Alarm2 from fan board RJ45 0: interrupt happened 1: not interrupt
[1]	ALARM1	R		Alarm1 from fan board RJ45 0: interrupt happened 1: not interrupt
[0]	ALARM0	R		Alarm0 from fan board RJ45 0: interrupt happened 1: not interrupt

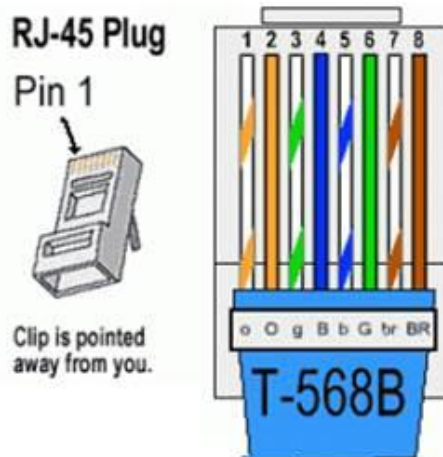
2.1.5.1.33 Offset 0x71 ALARM Relay Control (Read& Write)

Bit	Name	R/W	Reset Value	Description
[7:2]	Reserved			
[1]	Relay_NC_control	R/W	0	0: Relay contact CLOSED 1: Relay contact OPEN ***** Test pattern during functional test in production, test loop back cable is needed to alarm port. 0: ALARM4, ALARM3 = 0 1: ALARM4, ALARM3 = 1
[0]	Relay_NO_control	R/W	0	0: Relay contact OPEN 1: Relay contact CLOSED ***** Test pattern during functional test in production, test loop back cable is needed to alarm port. Need to with test cable. 0: ALARM2, ALARM1 = 1 1: ALARM2, ALARM1 = 0

(This is start from R0C use).



接線順序:
Pin 1 & 2 to 6
Pin 3 & 4 to 8
Pin 5 to 7



2.1.5.1.34 Offset 0x78 ALARM Mask (Read& Write)

Bit	Name	R/W	Reset Value	Description
[7:4]	Reserved	R/W		Reserved
[3]	ALARM3_mask	R/W	0	Mask for Alarm3 from fan board RJ45 0: no mask 1: mask enable
[2]	ALARM2_mask	R/W	0	Mask for Alarm2 from fan board RJ45 0: no mask 1: mask enable
[1]	ALARM1_mask	R/W	0	Mask for Alarm1 from fan board RJ45 0: no mask 1: mask enable
[0]	ALARM0_mask	R/W	0	Mask for Alarm0 from fan board RJ45 0: no mask 1: mask enable